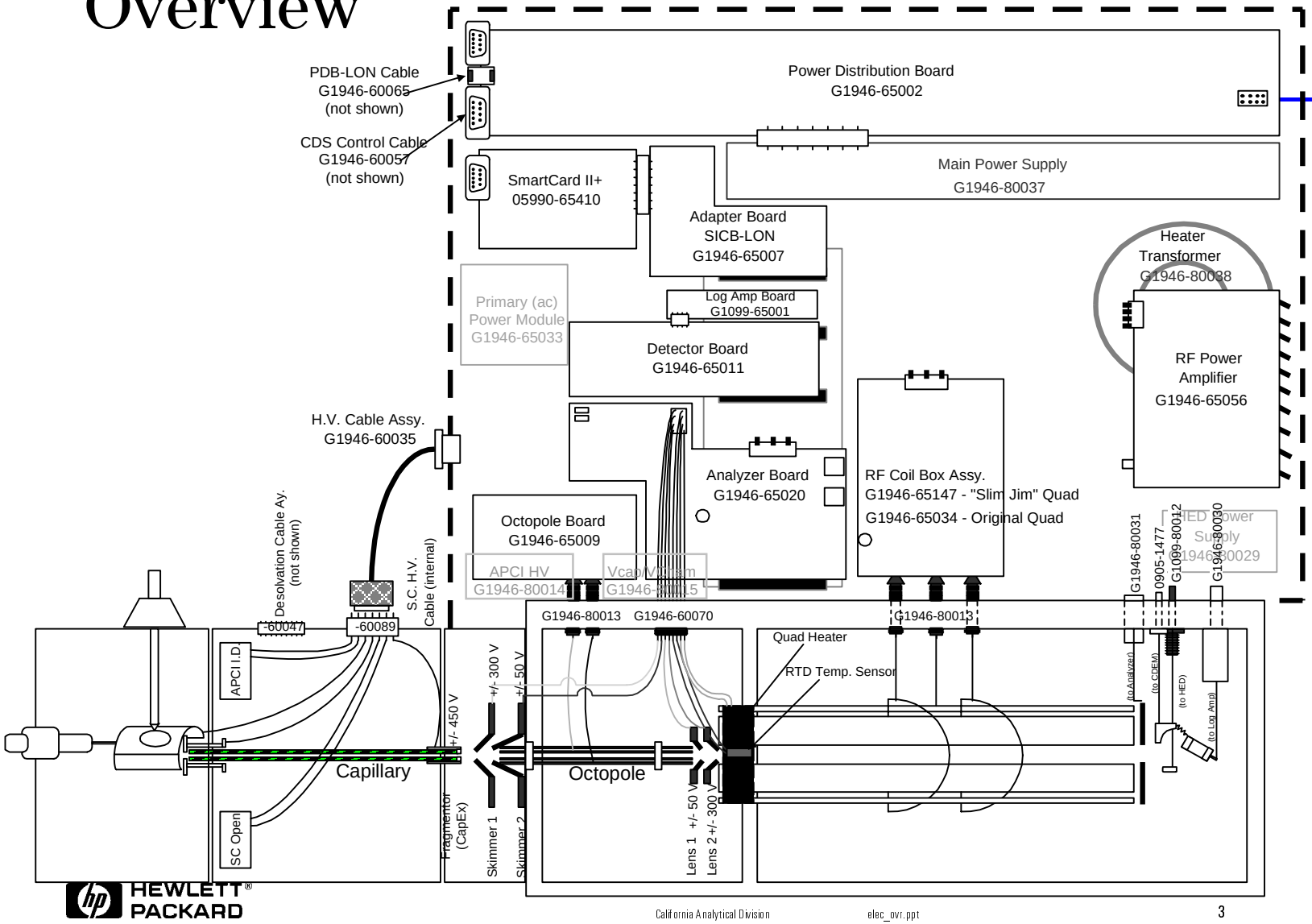
Electronics Overview

HEWLETT® PACKARD

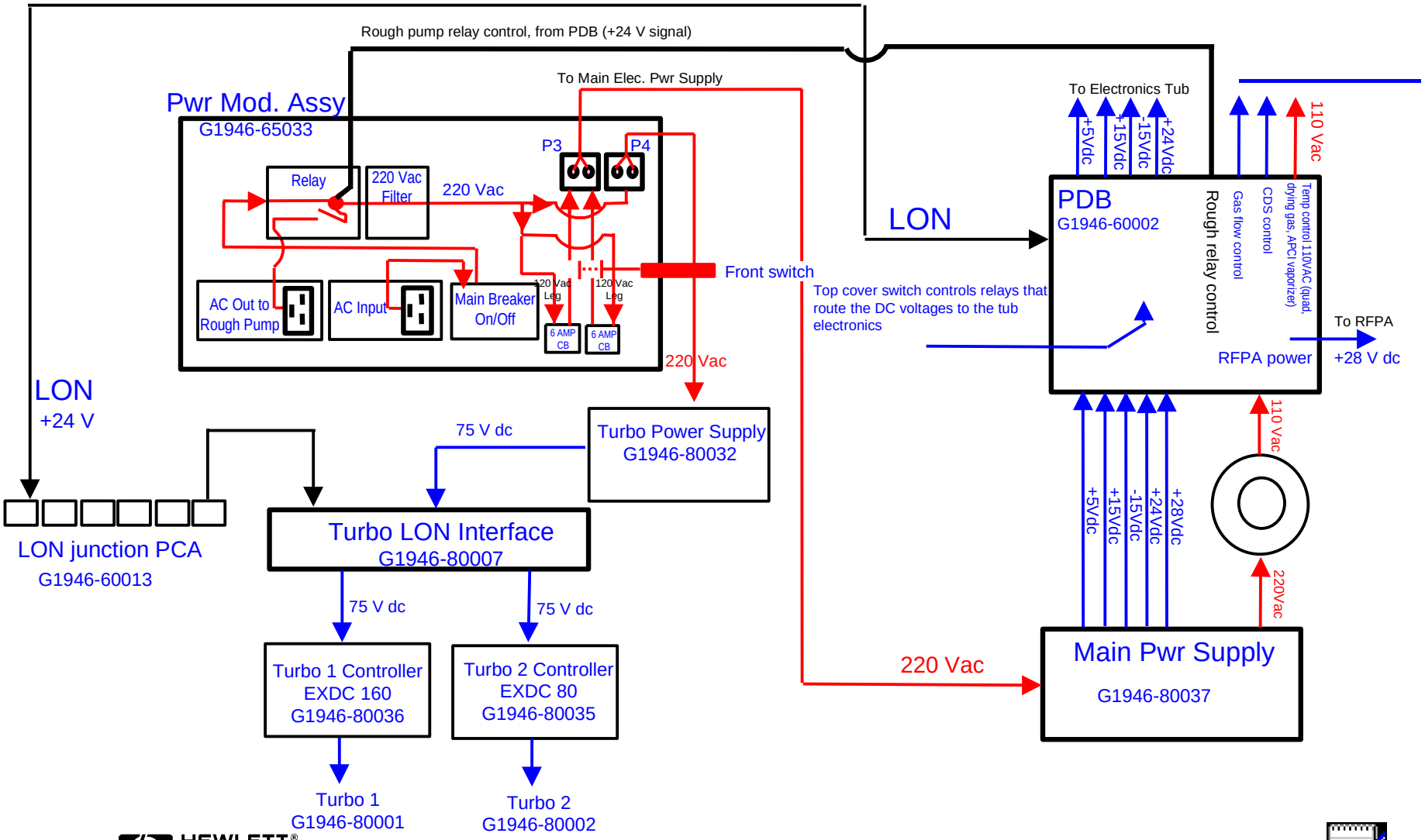
Objectives

- Identify the electronic assemblies used in the LC/MSD
- Describe the components of the Real Time and Non-Real Time Subsystem
- Identify cables and connectors used in the LC/MSD
- Describe the functions of the power distribution board
- Describe the functions of the analyzer board
- Identify test points and indicators on the electronic assemblies

Overview


PDB-LON Cable
G1946-60065
(not shown)
CDS Control Cable
G1946-60057
(not shown)
Power Distribution Board
G1946-65002
SmartCard II+
05990-65410
Main Power Supply
G1946-80037
Adapter Board
SICB-LON
G1946-65007
Heater
Transformer
G1946-80038
Primary (ac)
Power Module
G1946-65033
Log Amp Board
G1099-65001
Detector Board
G1946-65011
RF Power
Amplifier
G1946-65056
H.V. Cable Assy.
G1946-60035
Analyzer Board
G1946-65020
RF Coil Box Assy.
G1946-65147 - "Slim Jim" Quad
G1946-65034 - Original Quad
Octopole Board
G1946-65009
APCI HV
G1946-80014
Vcap/Vcham
G1946-80015
HED Power
Supply
G1946-80029
Desolvation Cable Ay.
(not shown)
S.C. H.V.
Cable (internal)
-60047
-60089
G1946-80031
0905-1477
G1099-80012
G1946-80030
G1946-80013
G1946-60070
G1946-80013
Quad Heater
RTD Temp. Sensor
(to Analyzer)
(to CDEM)
(to HED)
(to Log Amp)
APCI I.D
SC Open
Capillary
+/- 450 V
+/- 300 V
+/- 50 V
Fragmentor
(CapEx)
Skimmer 1
Skimmer 2
Octopole
Lens 1 +/- 50 V
Lens 2 +/- 300 V

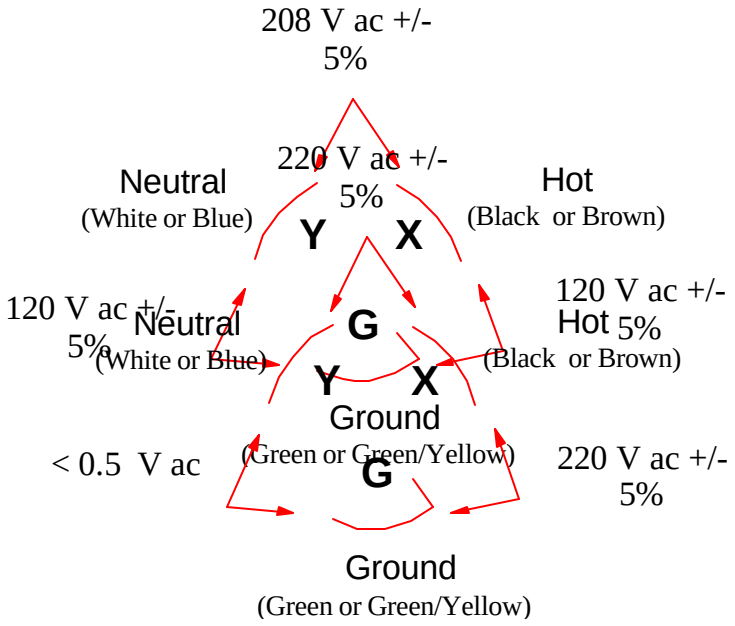
Front Switch & Main Breaker



Module: Electronics Overview
Page Tile: "Front Switch & Main Breaker"
Page #: 4
Last Revised: 12/23/98

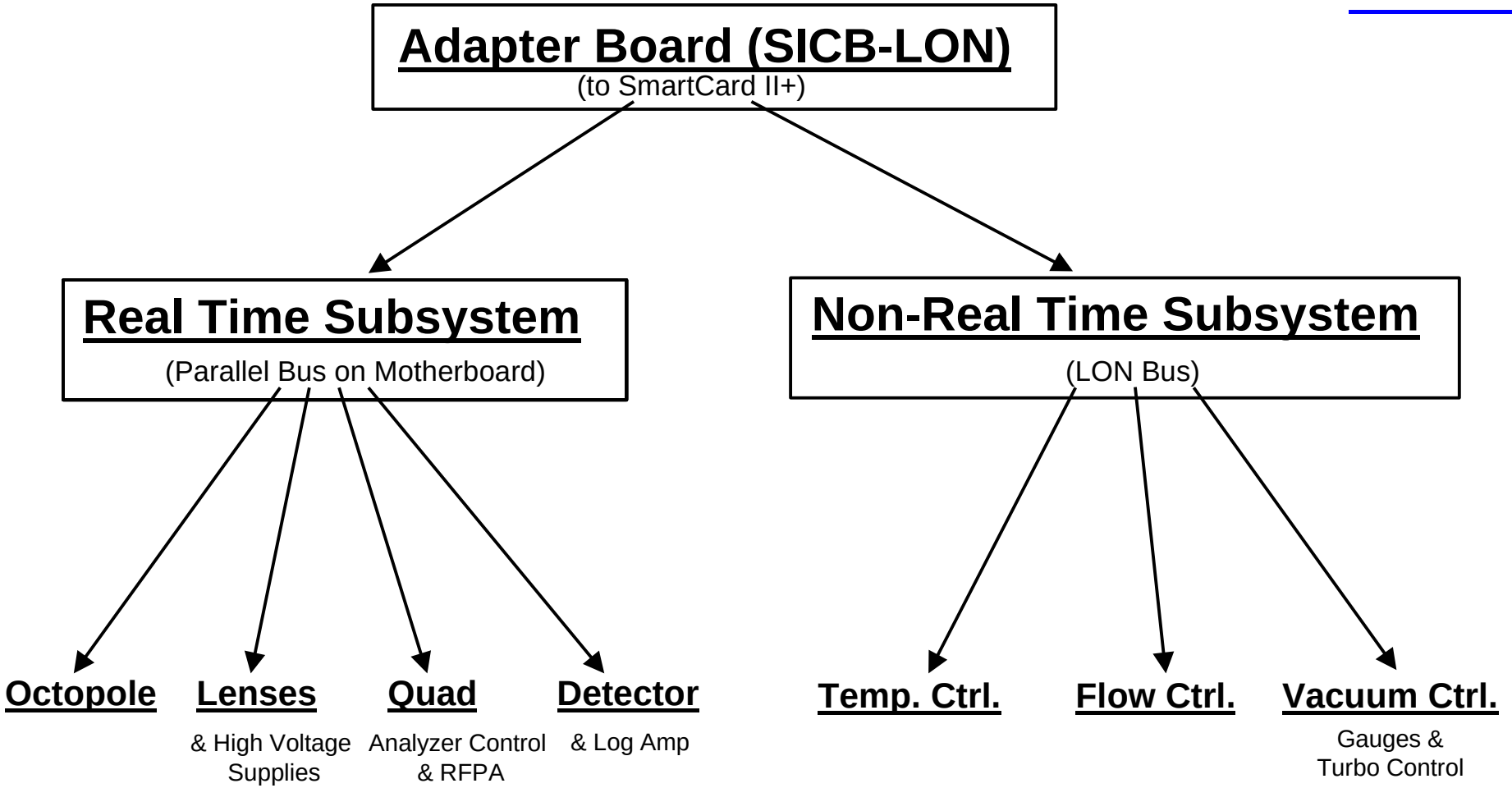
This drawing is slightly inaccurate by showing the P3 Circuit Breaker supplying 220VAC to the Main Electronics Supply, and the P4 Circuit Breaker supplying 220VAC to the Turbo Power Supply. Actually, each circuit breaker handles one leg of the 120VAC (Y to G and X to G) for the 208 Wye Configuration (see below). This is to protect against a ground fault (short) to either leg.

208 Wye Configuration

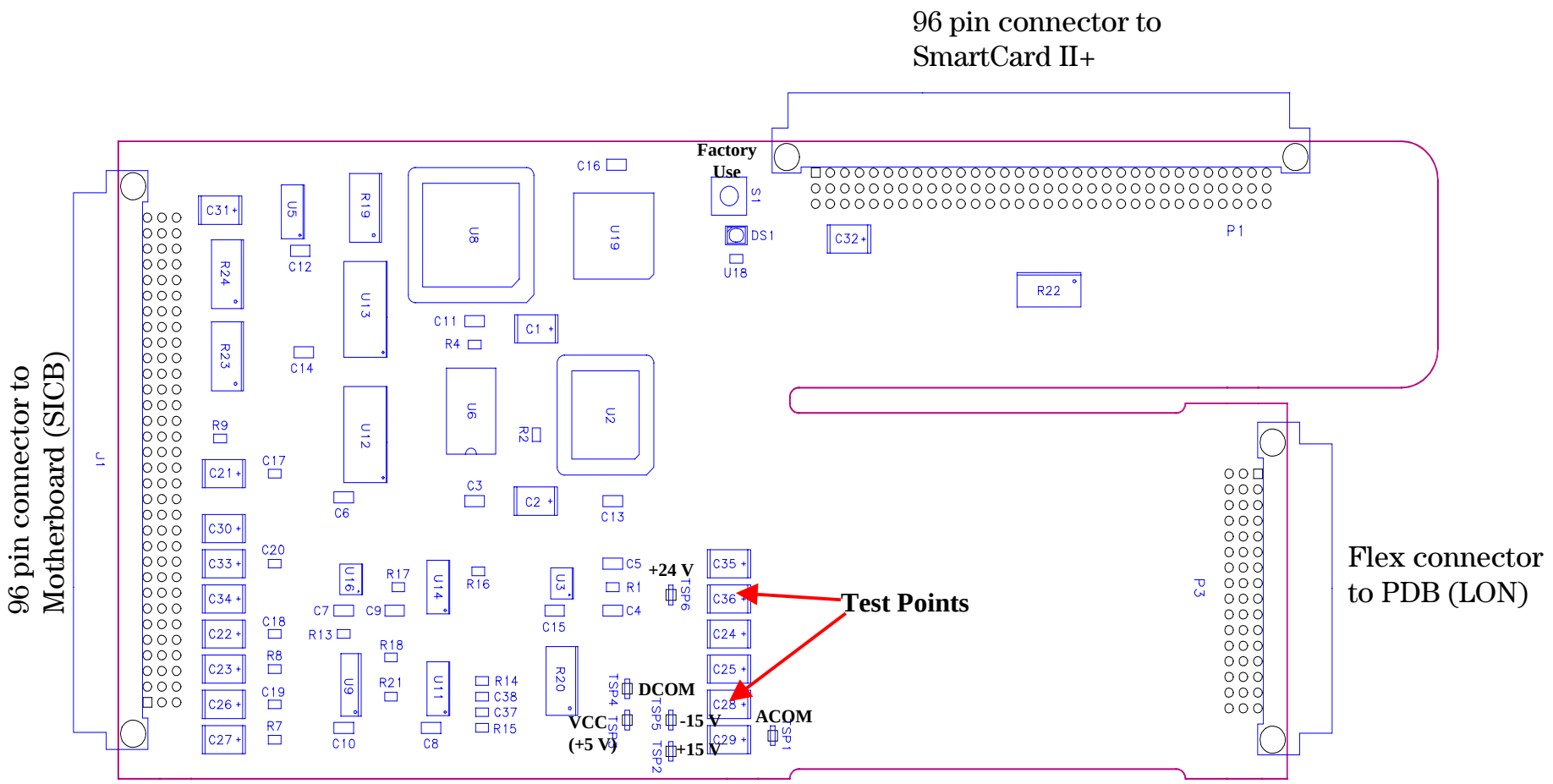


220V Single Phase

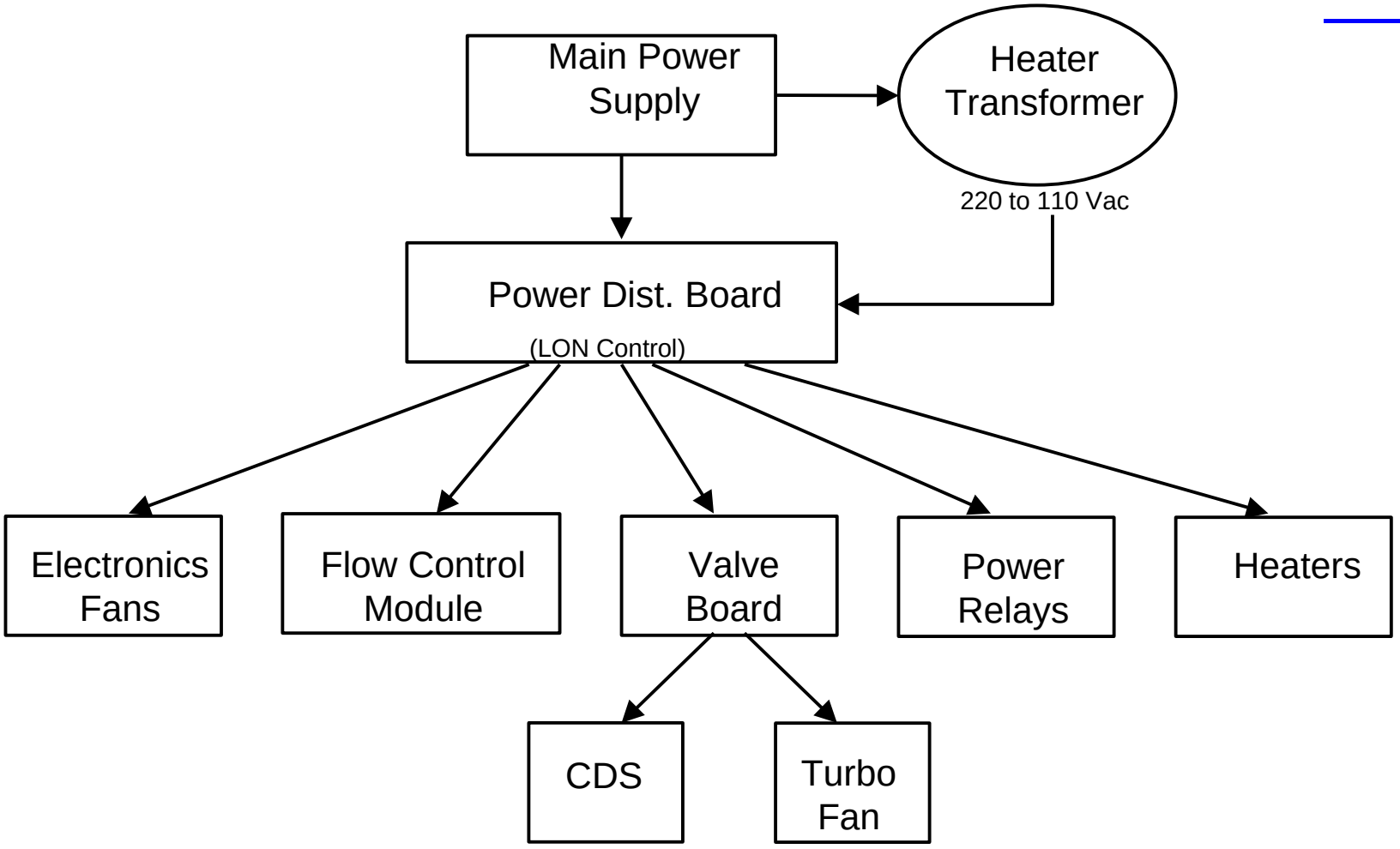
SICB-LON Control Overview



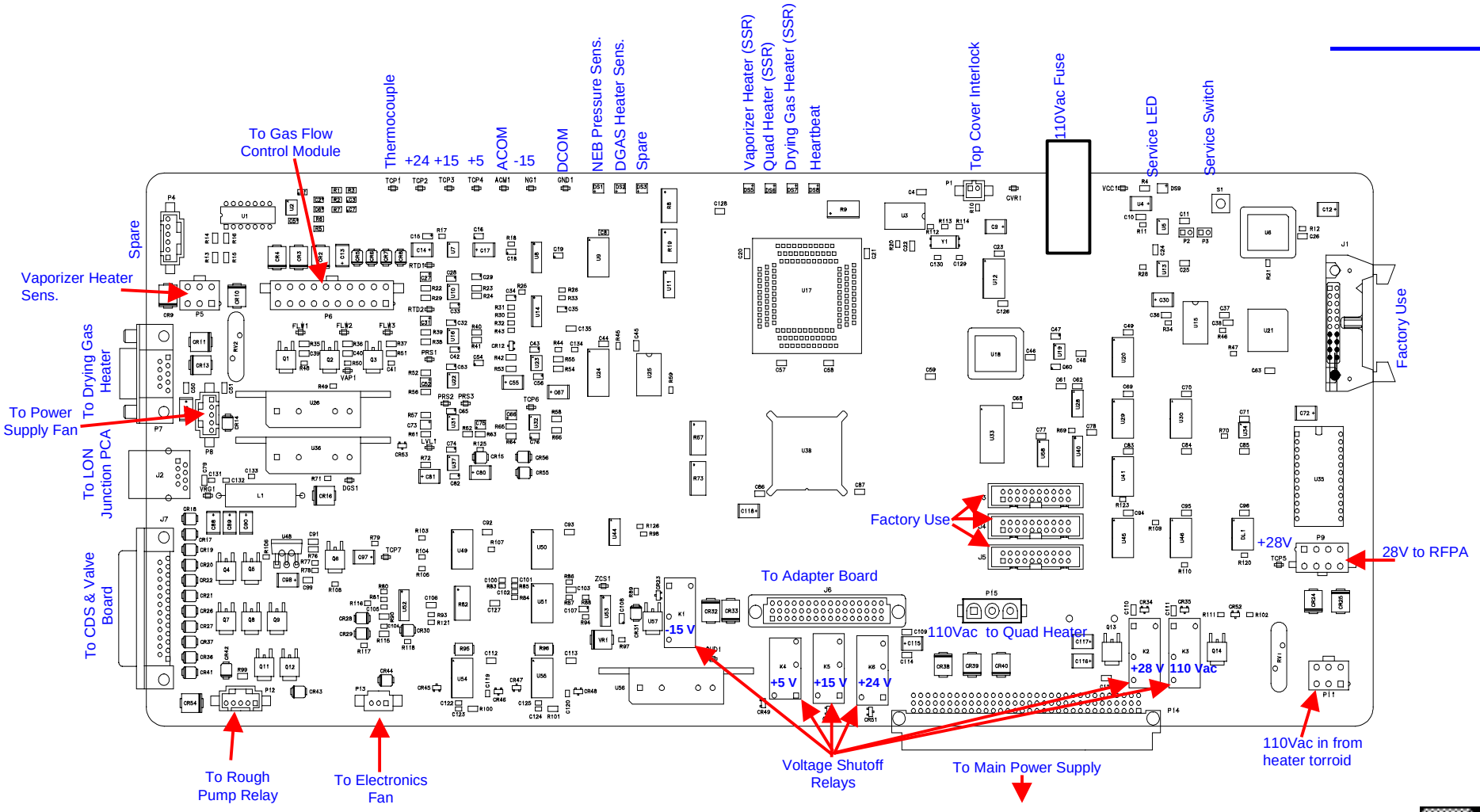
Adapter Board (SICB-LON)



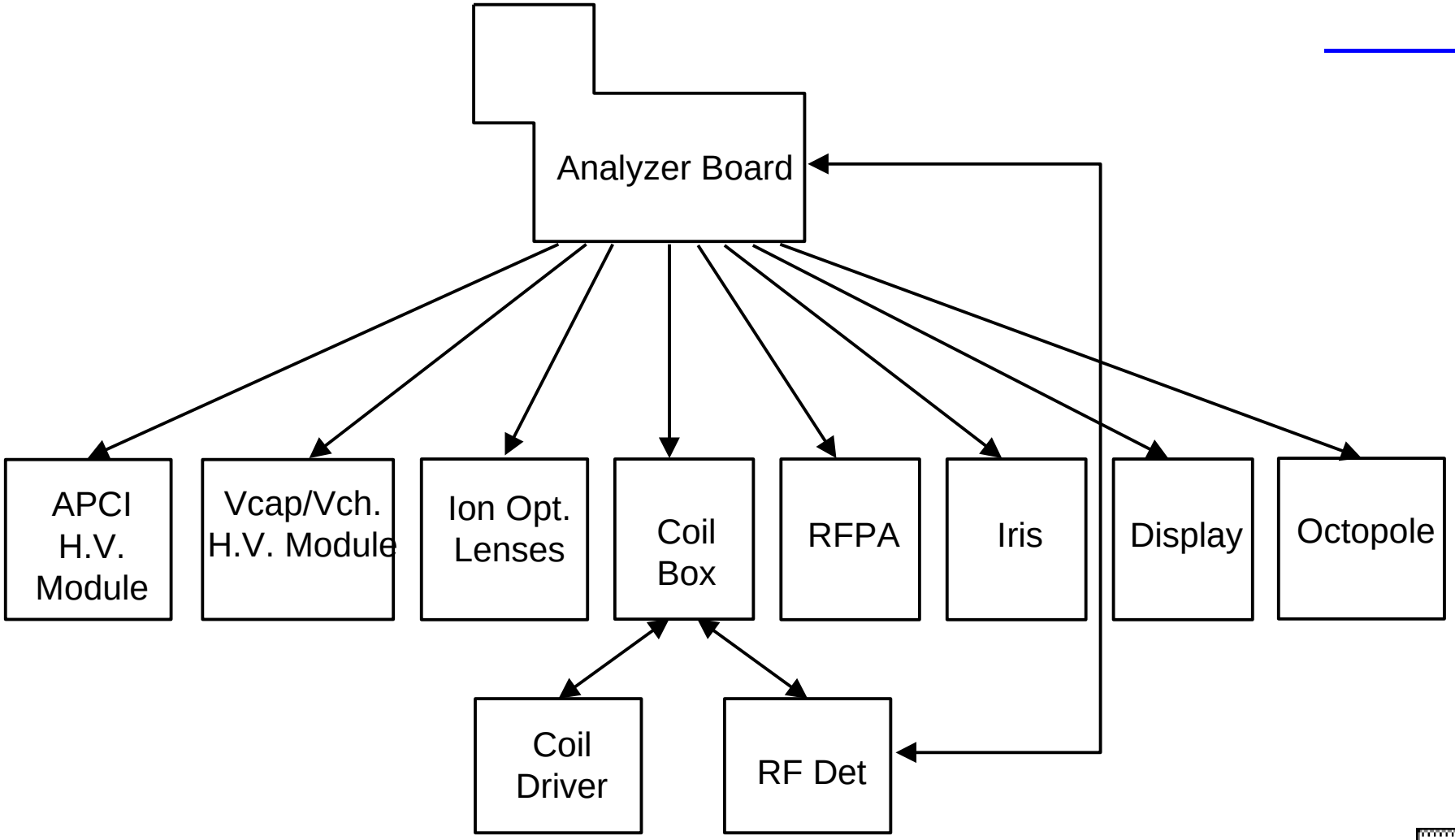
PDB Control Overview



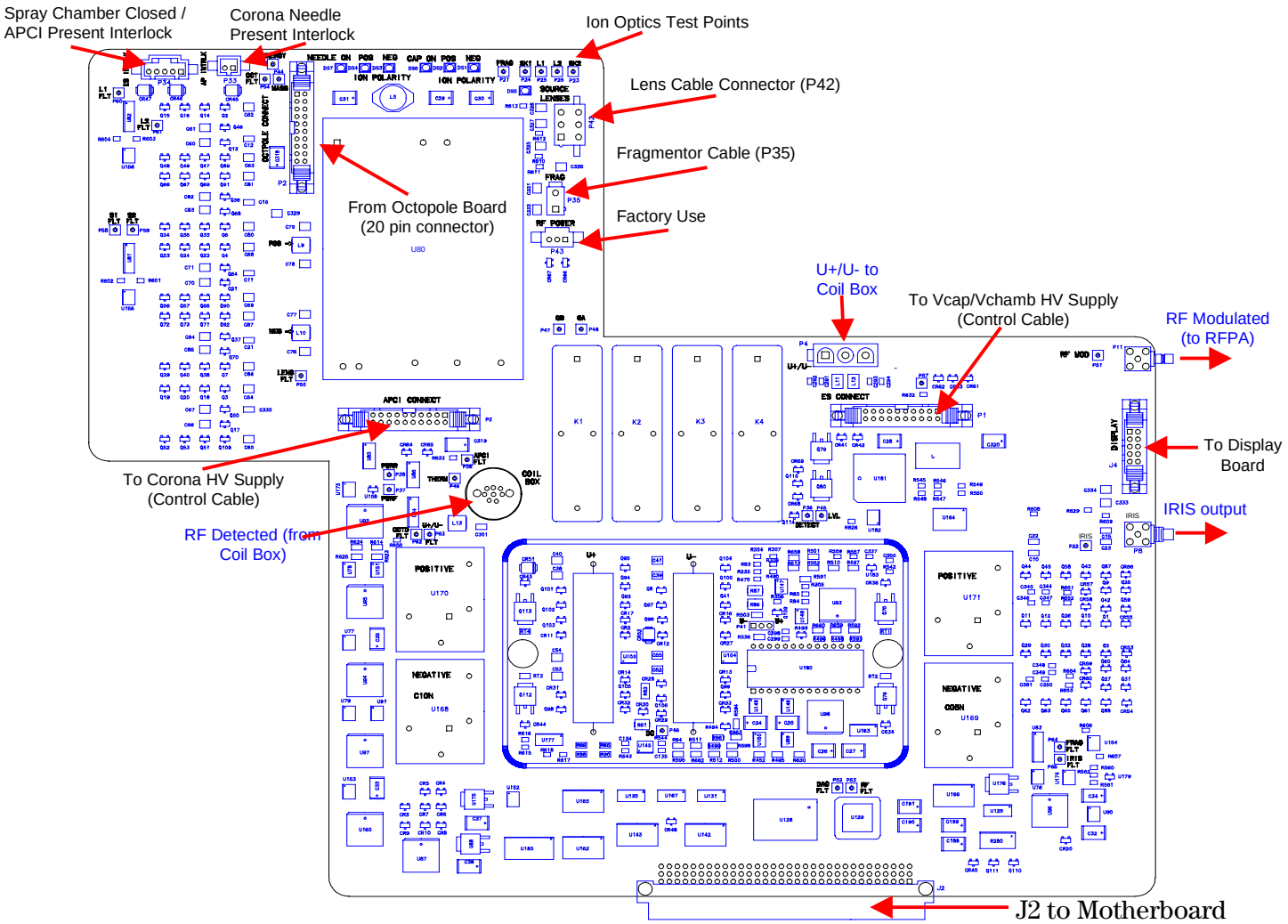
Power Distribution Board (PDB)



Analyzer Board Modules



Analyzer Board



Analyzer Board

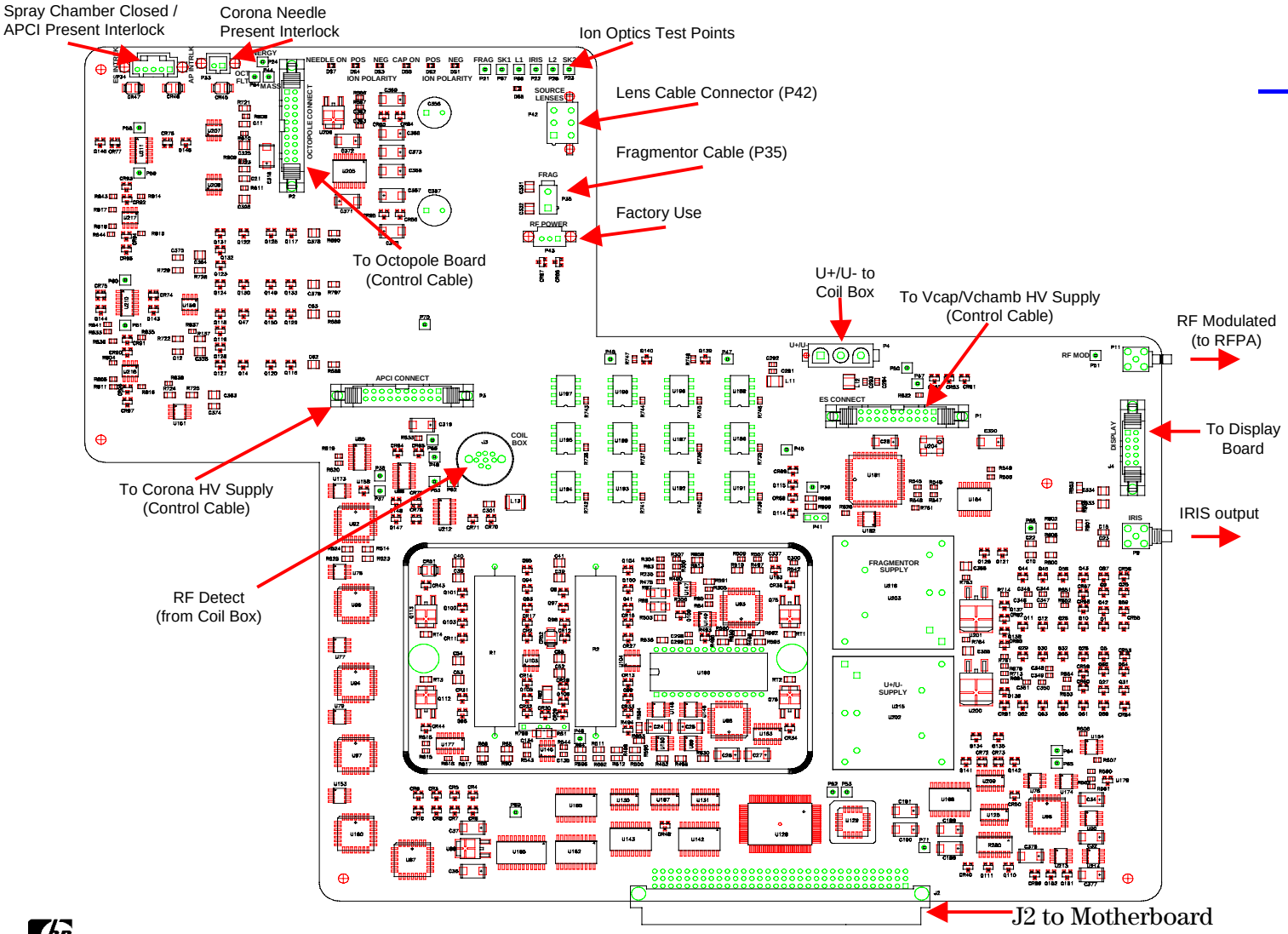
Part Numbers

G1946-65001	Tested Analyzer Board
G1946-69001	Rebuilt Analyzer Board
G1946-65020	Tested Analyzer II Board
G1946-69020	Rebuilt Analyzer II Board

As shown by the previous slide, this board controls the Real Time Subsystem parameters. The -65001 and -69001 Analyzer Boards were prone to "Quad DC" or "Ion Optics Fault 4" error messages associated with the U+/U- power supplies. These power supplies were replaced with different supplies on the Analyzer II Board, G1946-6x020.

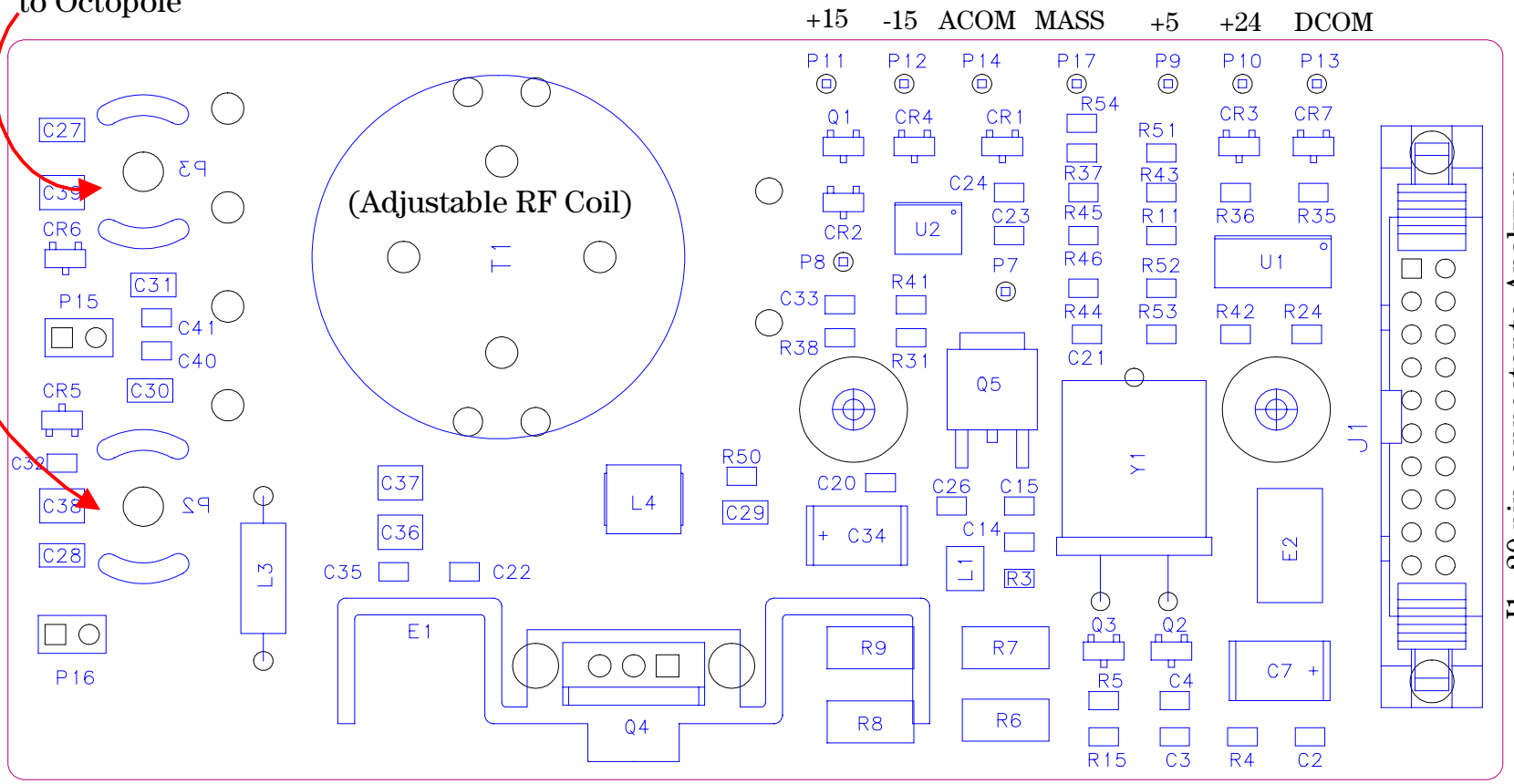
See Analyzer II Board.

Analyzer II Board



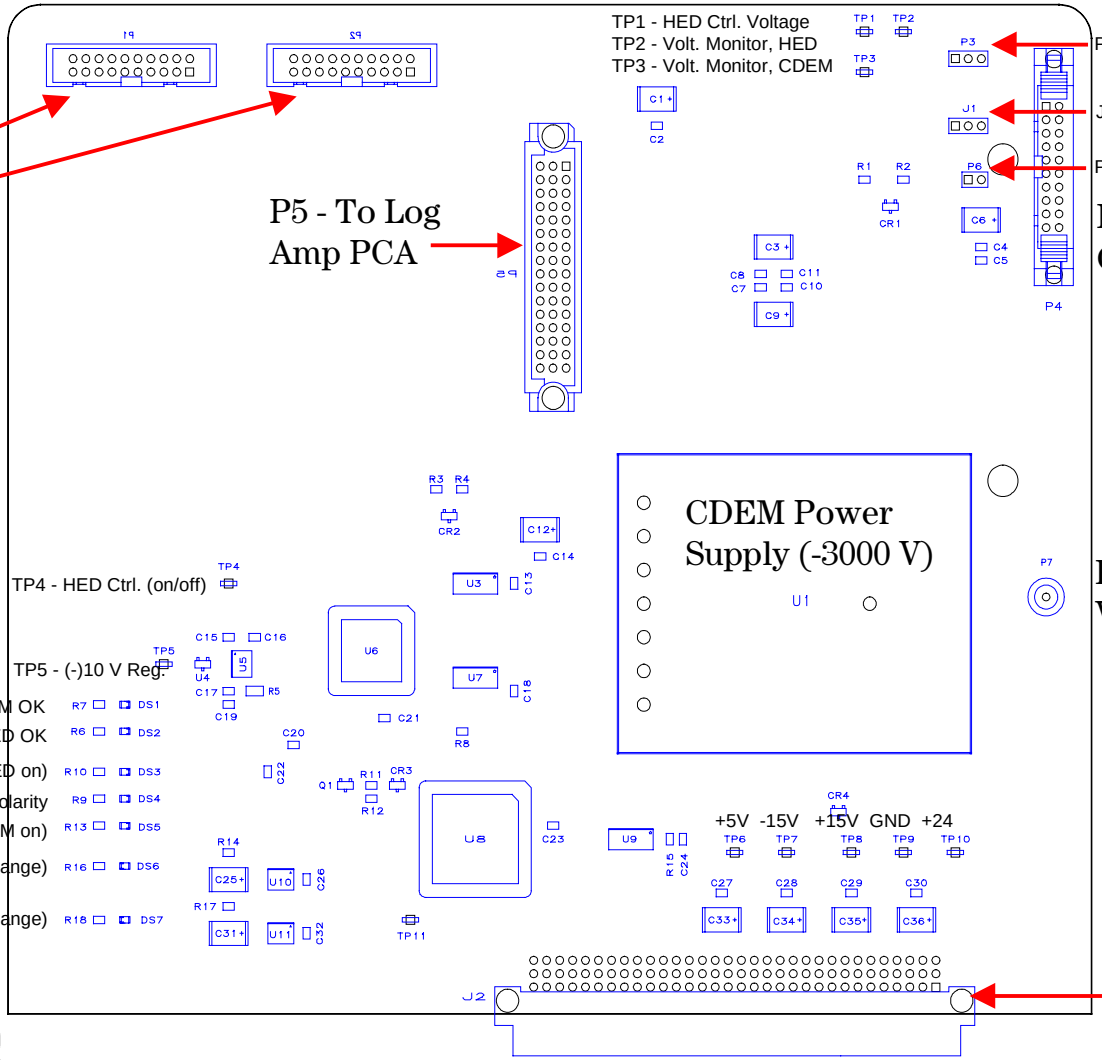
Octopole Board

P2 & P3 - RF feedthroughs to Octopole



J1 - 20 pin connector to Analyzer Board (ribbon cable)

Detector Board



P1 & P2 - Board Logic Analyzer Connections (Factory Use Only)

P5 - To Log Amp PCA

P3 - K&M Jumper #1

J1 -Gamma HED Jumper

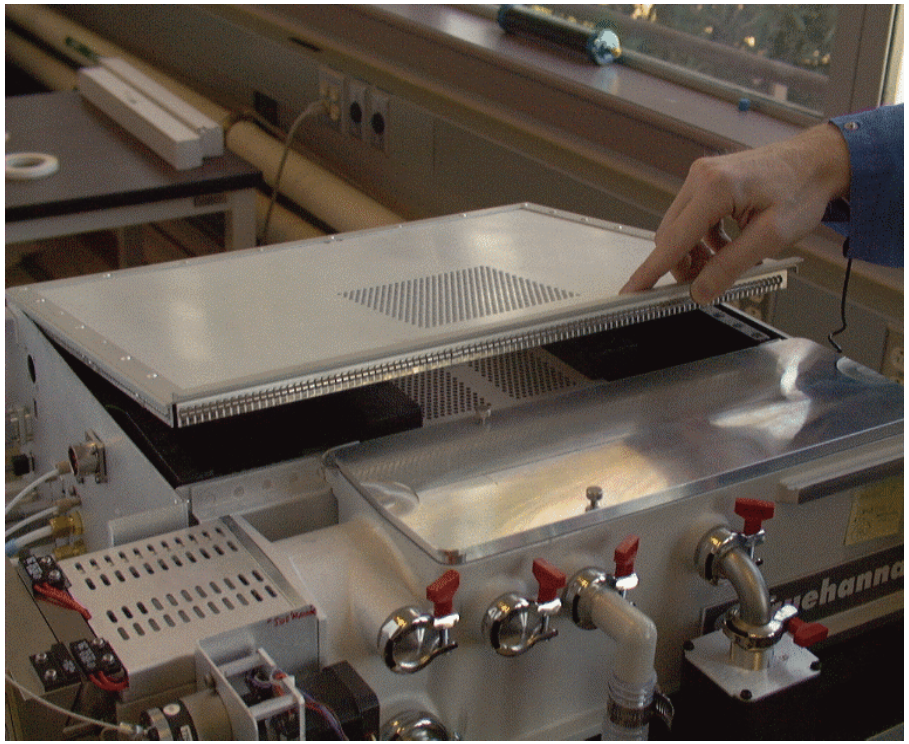
P6 - K&M Jumper #2

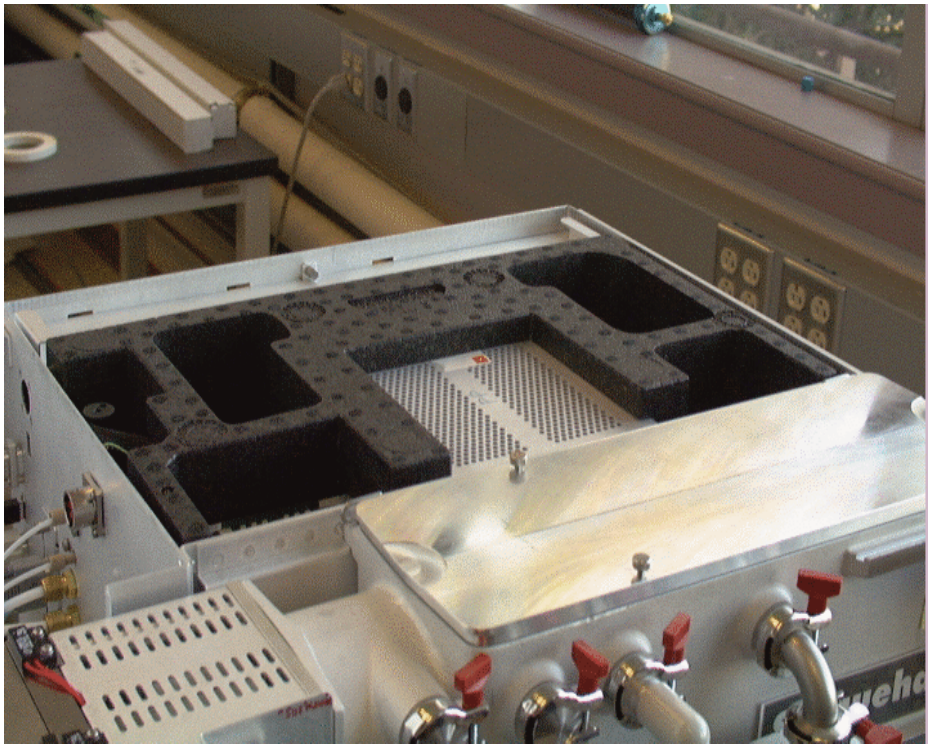
P4 - HED Control Cable

P7 - CDEM High Voltage Cable

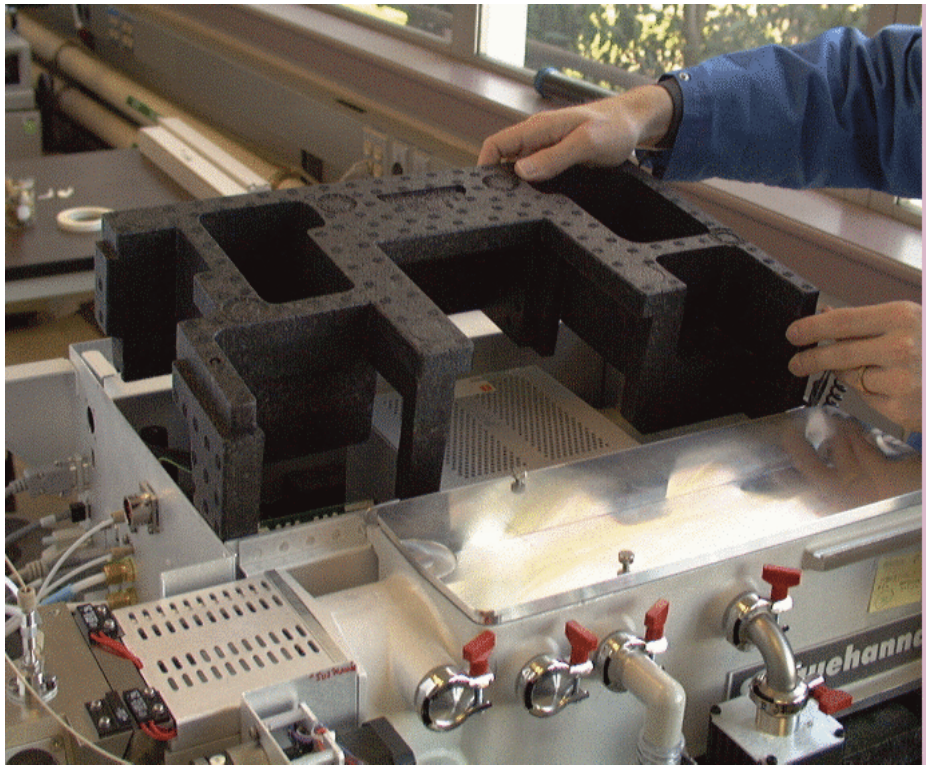
J2 - 96 pin connector to Motherboard

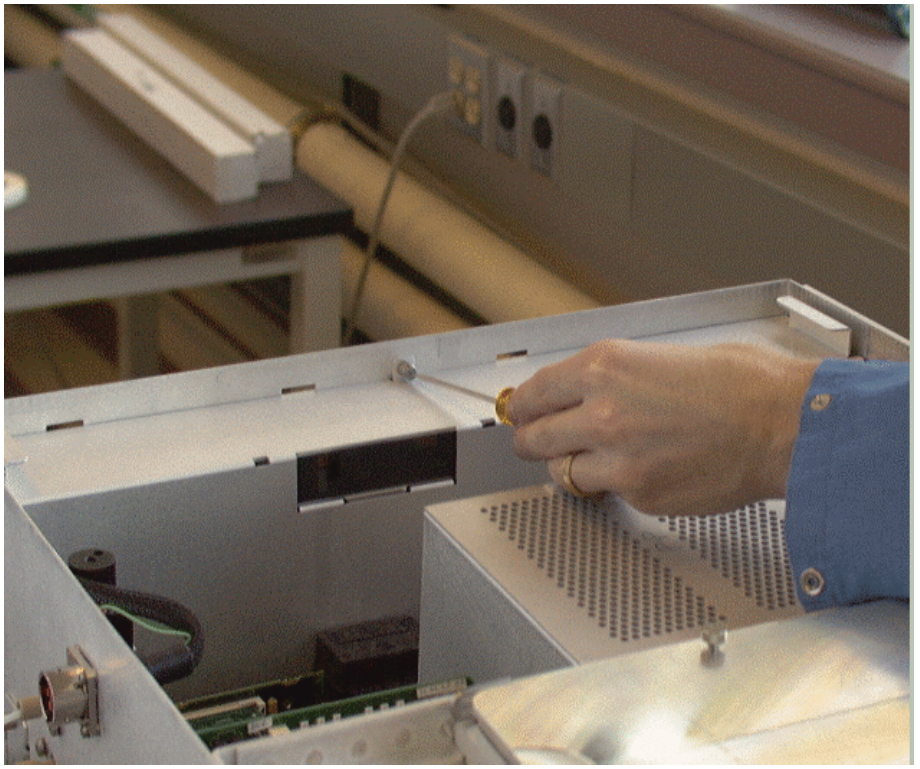
Removing Top Cover



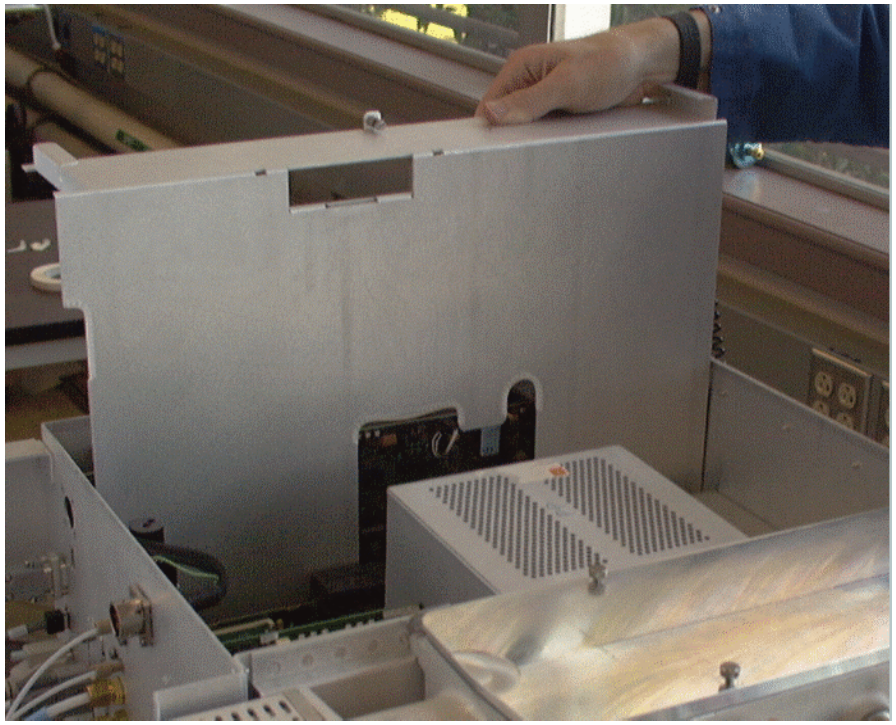


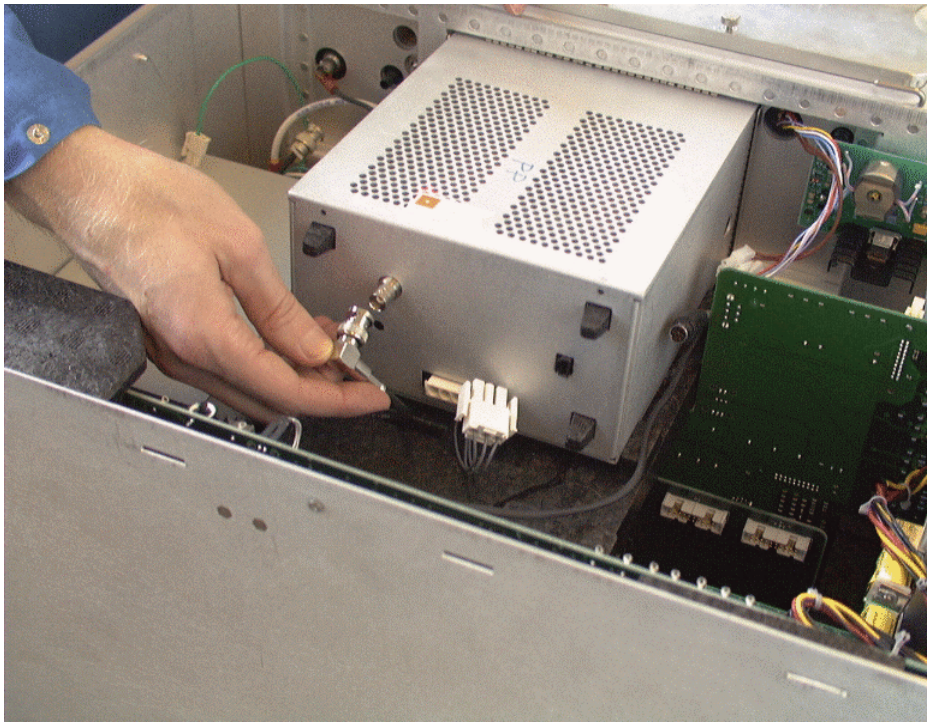
Removing E-PAC Foam Top Piece + Removing Electronics Cover



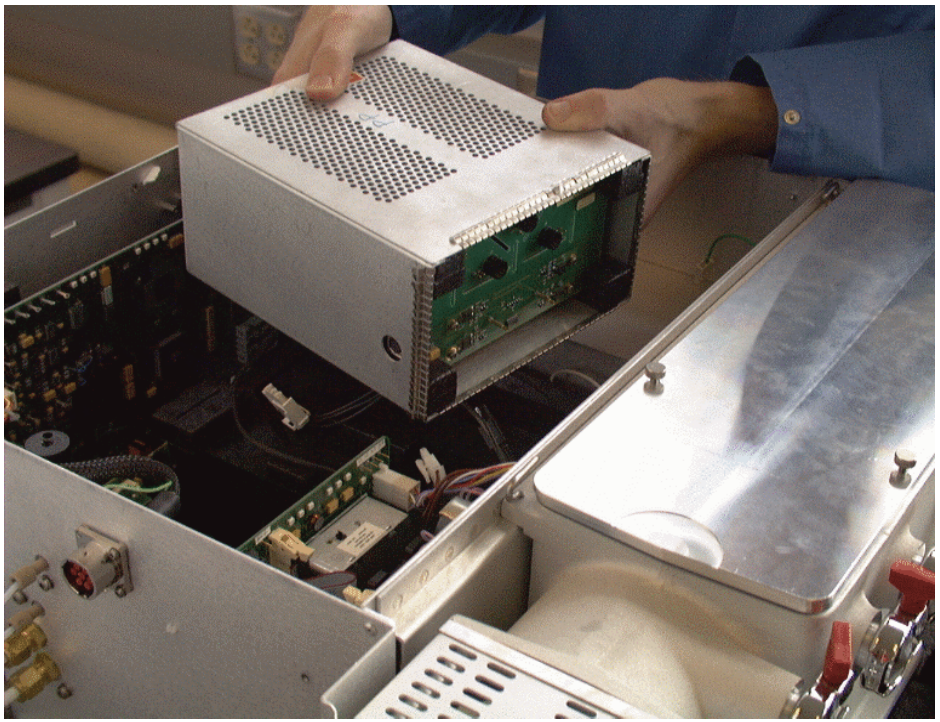


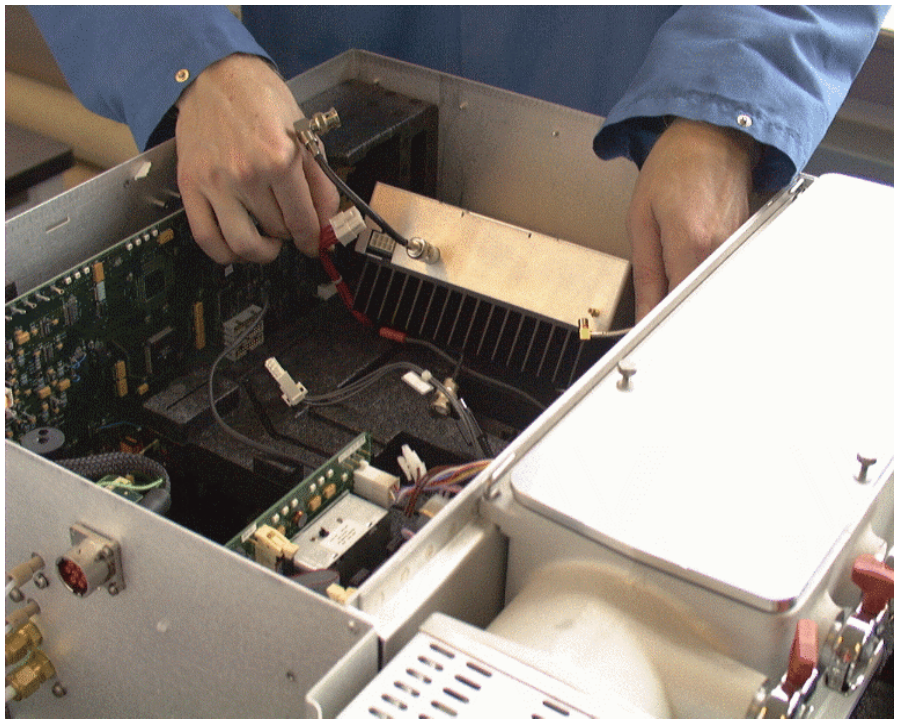
Removing Electronics Cover + Disconnecting RF Leads



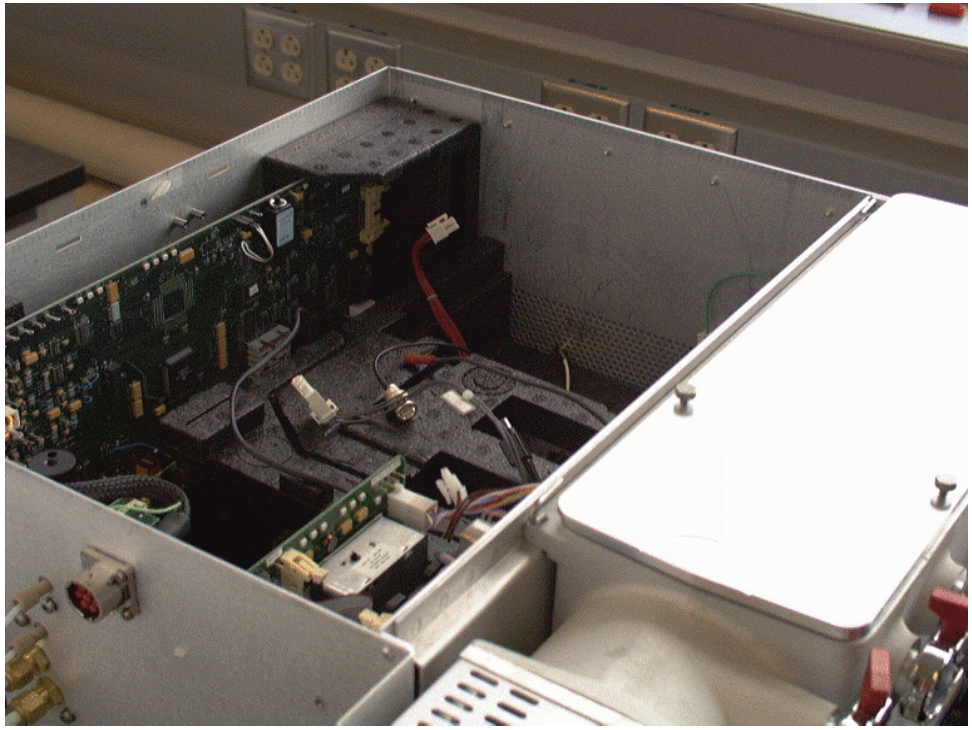


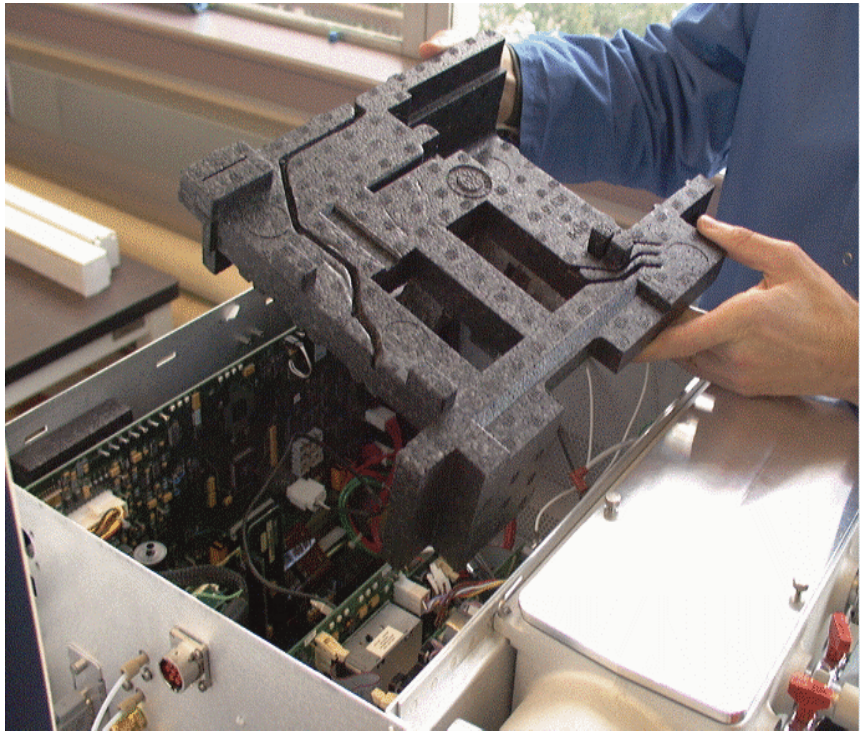
Removing RF Coil Box
+ Removing RF Power Amplifier



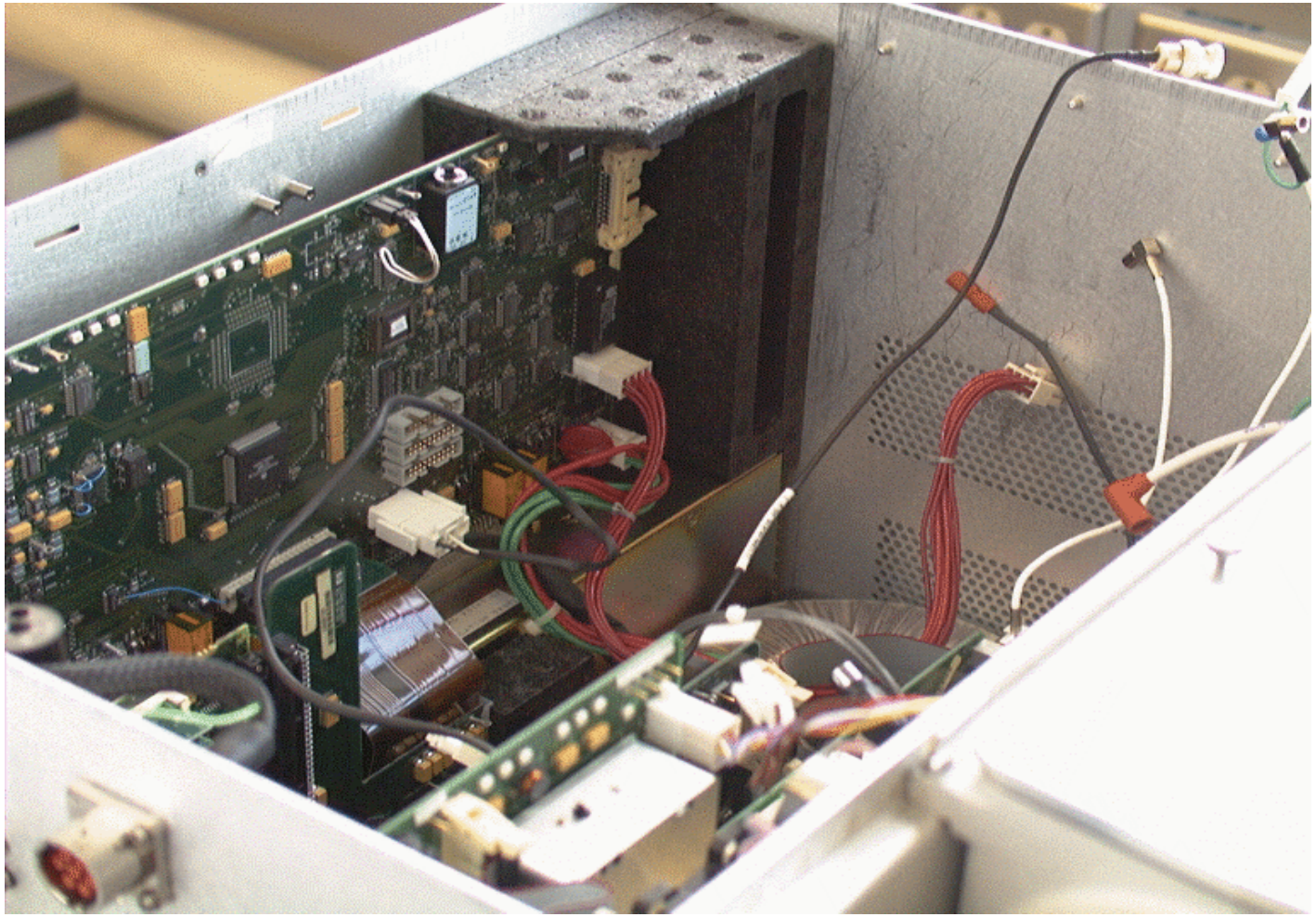


Removing Middle E-PAC Foam Piece





Electronics Tub



Location of Non-Volatile RAM Parameters

There are numerous non-volatile parameters stored in the LC/MSD. From time to time, these may disappear or get changed, causing some very serious problems.

There are two common causes of loss of non-volatile parameters: 1) Replacement of the part that holds the value; and 2) Loading an earlier revision of SmartCard code. If SmartCard code is downloaded, and a later revision is found, then all of the non-volatile RAM on SmartCard is cleared. This causes the LC/MSD to lose its quad polarities, quad frequency, gain curve, and a bunch of other items.

Other parameters will be lost if either the SmartCard, SICB/LON adapter or PDB are changed. The list below shows which values (taken from the ShowNVR report) are found on which board. This report is generated using the CE Utility macro ShowNVR.mac.

Non-Volatile RAM Parameter	Location
Serial Number	SICB/LON
Product Number	SICB/LON
Mfg Date	SICB/LON
Quad Serial Number	SICB/LON
MS Inject Valve Present	SmartCard
ChemStation Rev	ChemStation SW
SmartCard Rev	ChemStation SW
PDB HW Rev	PDB
PDB FW Rev	PDB
PDB 68332 FW Rev	PDB
SICB-LON HW Rev	SICB/LON
SICB-LON FW Rev	SICB/LON
Turbo Pump Ctrl HW Rev	Turbo/LON interface
Turbo Pump Ctrl FW Rev	Turbo/LON interface
Convect. Gauge HW Rev	Convectron gauge
Convect. Gauge FW Rev	Convectron gauge
Ion Gauge HW Rev	Ion gauge
Ion Gauge FW Rev	Ion gauge
Log Amp ID	Detector board
Quad Frequency	SmartCard
Pos Ion Quad Polarity	SmartCard
Neg Ion Quad Polarity	SmartCard
Stdby Quad Temp	SmartCard
Stdby Drying Gas Temp	SmartCard
Stdby Drying Gas Flow	SmartCard
Stdby Nebulizer Press	SmartCard
Stdby Vaporizer Temp	SmartCard
Quad Temp PIDs	PDB
Drying Gas Temp PIDs	PDB
Vaporizer Temp PIDs	PDB
Drying Gas Flow PIDs	PDB
Nebulizer Pres PIDs	PDB

Quad Temp Timeout	PDB
Drying Gas Temp Timeout	PDB
Vaporizer Temp Timeout	PDB
Drying Gas Flow Timeout	PDB
Nebulizer Pres Timeout	PDB
CDS Leak Sensor Calibration	PDB
CDS On Purge Time	SmartCard
CDS Off Purge Time 1	SmartCard
CDS Off Purge Time 2	SmartCard
CDS On Delay	SmartCard
Mass Axis Lag D Coeff 0	SmartCard
Mass Axis Lag D Coeff 1	SmartCard
Mass Axis Lag D Coeff 2	SmartCard
Std EMV	Calculated
EMV Gain Coeff 0	SmartCard
EMV Gain Coeff 1	SmartCard
EMV Gain Coeff 2	SmartCard
EMF limit: Calibrant A hrs	SmartCard
EMF limit: Calibrant B hrs	SmartCard
EMF limit: Pump Oil hrs	SmartCard
EMF limit: Gas Conditioner hrs	SmartCard
EMF limit: Ion Optics hrs	SmartCard
EMF limit: SSV Cycles	SmartCard
EMF limit: EM Current	SmartCard

Adjustments Required When Replacing Electronic Boards

When You Replace The…	You Need To…
Analyzer Board (G1946-65001)	1. Adjust the quad frequency (select "MSD Frequency Adjustment" from the Maintenance menu in Diagnosis view) 2. Adjust the output of the RFPA (see "RFPA Adjustment Procedure" in Mass Filter section)
Power Distribution Board (G1946-65002)	1. Perform a CDS leak sensor calibration (see "Calibrating and Verifying Operation of CDS Leak Sensor" in CDS & Manual Inj. Valve section)
Adapter Board (G1946-65007)	1. Reenter NVRAM parameters: LC/MSD serial number, product number, MFG date, quad serial number (type SetNVR on the command line. See "CE Utility Macros" in Diagnostics & Troubleshooting section)
Octopole Board (G1946-65009)	1. Dip the octopole assy (see "Octopole Board Dipping Procedure" in the Source & Ion Optics section)
Detector Board (G1946-65011)	No adjustments necessary
RF Coil Box (G1946-65147/ G1946-65034)	1. Adjust the quad frequency (select "MSD Frequency Adjustment" from the Maintenance menu in Diagnosis view) 2. Adjust the output of the RFPA (see "RFPA Adjustment Procedure" in Mass Filter section)
RFPA (G1946-65056)	1. Adjust the quad frequency (select "MSD Frequency Adjustment" from the Maintenance menu in Diagnosis view) 2. Adjust the output of the RFPA (see "RFPA Adjustment Procedure" in Mass Filter section)
SmartCard II+ (05990-65410)	1. Burn the preferred quad polarity (see "How to Change the Quad Polarities on the LC/MSD" in the Mass Filter section) 2. Adjust the quad frequency (select "MSD Frequency Adjustment" from the Maintenance menu in Diagnosis view) 3. Burn the MS Injection Valve configuration, if present (see the "HP G1949A Manual Injection Valve Installation Manual", step #9, in the CDS & Manual Inj Valve section) 4. Perform an autotune to reestablish the emv gain curve 5. Reestablish the mass axis lag factors (type Set_Lag on the command line. See "CE Utility Macros" in Diagnostics & Troubleshooting section)
HED Power Supply (G1946-80029)	No adjustments necessary
Main Power Supply (G1946-80037)	No adjustments necessary
Log Amp Board (G1099-65001)	No adjustments necessary

Theory of Operation

HEWLETT PACKARD

HEWLETT-PACKARD
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Palo Alto, California 94304

REV	REVISIONS	APPROVED	DATE
A	AS ISSUED PER PC23-6030	N. Moreyra	08/01/97
B	Revised per PC23-6391	B. Capriles	01/15/97

Rev B: Modified sections 5.4.1, 5.4.2, and 5.5.1. Added conversion from DAC to host sofware setting.

Table of Contents

1.0 Introduction

The assembly, G1946-60001, is referred to as the Analyzer board. Its main goal is to control all the source elements, the octopole, the quad, and the display board. The board also provides a lot of status information relative to the elements it controls. The source elements include control of the APCI corona, capillary & chamber voltages, and lens voltages. The octopole control functions are the set points for RF peak-to-peak voltage and Knee voltage. The quad functions include the U+/U- DC voltages, the RF control voltages, and the quad frequency. The display board control functions are signals driven to the display board to control the blinking and color combinations.

2.0 Functional Specification

This section will list a summary of all of the relationships on the board. This is most useful to those who need to know the relationships in order to develop code or macros to control the instrument. It seemed best to put the summary list at the beginning of the document. Sections throughout this document will show the derivations of the relationships.

Table 1: Functional Specification

Parameter	Address	Range	Resolution	Relationship
Mass Axis	164 high, 36 low byte	0 to 3276.75 AMU	0.05 AMU	DAC = 20 * AMU
Mass Offset	29	-4.094 to +4.096 AMU	0.002 AMU	DAC = 2048 + 500 * AMU
Mass Gain	38	-102.4 to +102.35 AMU @ 3276.8 AMU	0.05 AMU @ 3276.8 AMU	DAC = 2048 + 20 * AMU
AMU Offset	21	-2047 to +2048 #	1 #	DAC = 2048 - #
AMU Gain	37	-2047 to +2048 #	1 #	DAC = 2048 - #
Quad DC	30	-39.98 to +40 volts	0.02 volts	DAC = 2048 - 50 * volts
Quad Frequency	144 data, 145 control	DC to 20 Mhz	4.7 millihertz	Count = $2^{\wedge 32}$ * (Freq[Khz]/20000)
Opole RF Peak	66	0 to 300 v P-P	0.125 mvolt	DAC = 8 * volts
Opole Knee	67	0 to 3276 AMU	1 AMU	DAC = AMU
Fragmentor	131	-425v to +425v	0.25 volt	DAC = 2048 + 4 * volts
Skimmer1	134	-250v to +250v	0.25 volt	DAC = 2048 + 4 * volts
Skimmer2	135	-51.2v to +51.175v	0.025 volts	DAC = 2048 + 40 * volts
Ion Energy	136	-51.2v to +51.175v	0.025 volts	DAC = 2048 + 40 * volts
Lens1	132	-51.2v to +51.175v	0.025 volts	DAC = 2048 + 40 * volts
Lens2	133	-250v to +250v	0.25 volt	DAC = 2048 + 4 * volts
Iris	28	-425v to +425v	0.25 volt	DAC = 2048 + 4 * volts
Capillary	128	-6000v to +6000v	50 volts	DAC = volts/2.4420

Table 1: Functional Specification

Parameter	Address	Range	Resolution	Relationship
Corona Current Neg. APCI All other modes	130	 0 to 100uA 0 to 10uA	 0.1 uA 0.1 uA	 DAC = 40.96 * current[uA] DAC = 409.6 * current[uA]
APCI Current Readback Neg. APCI Pos. APCI	34, channel 8	 0 to 100 uA 0 to 10 uA	 0.392 uA 0.0392 uA	 Value[uA] = 0.392 * A/D Value[uA] = 0.0392 * A/D
Vcap Voltage Readback	34, channel 9	0 to 10 KV	0.0392 KV	Value[KV] = 0.0392 * A/D
RF Drive Level Readback	34, channel 10	0 to 100 %	0.3922%	Value[%] = 0.3922 * A/D
CAP Current Readback	34, channel 11	0 to 2 uA	7.8 nA	Value[nA] = 7.84 * A/D
Chamber Current Readback Neg. APCI All other modes	34, channel 12	 0 to 100 uA 0 to 10 uA	 0.392 uA 0.0392 uA	 Value[uA] = 0.392 * A/D Value[uA] = 0.0392 * A/D
APCI Voltage Readback	34, channel 13	0 to 6 KV	39.2 volts	Value[KV] = 0.0392 * A/D
RF Forward Pwr Readback	34, channel 14	0 to 100 Watts	0.392 Watts	Value[W] = 0.392 * A/D
RF Reflected Pwr Readback	34, channel 15	0 to 100 Watts	0.392 Watts	Value[W] = 0.392 * A/D
Status1	0	N/A	N/A	16 bit readback
Status2	1	N/A	N/A	16 bit readback
Identification	2	N/A	N/A	16 bit Identification value
Shutdown Mask	6	N/A	N/A	16 bit Mask for Status1
Mode Control	137	N/A	N/A	16 bit Mode Control word
Dummy Lens	255	N/A	N/A	DO NOT USE

All of the elements in the above table are controlled by the Analyzer board. The values for range and resolution represent the hardware functionality. Software may want to limit the ranges and have coarser resolutions to make the functions more user friendly.

3.0 Schematics

There are 18 pages of schematics for the board design of the Analyzer board. The pages are grouped together to describe various functions of the board. The best way to understand the following description is to have the schematics on hand. There is one Field Programmable Gate Array (FPGA) on the board that has 5 schematic pages. It would be advisable to get the associated design documents for this FPGA, G1946-80053, to help understand the control functions of the board.

3.1 Page 1 of 18, Top Level

The first page of the schematic is a high level block description of the design. In the MENTOR environment, the design is broken into 4 functional areas. Each area has numerous schematic pages and a symbol page. The symbols are brought together on this first page to link the 4 functional modules together. The first symbol is the *Mass Axis Control and U+/U- Amplifier* function. This area consists of schematic pages 2 through 5. The second symbol is the *MSE Interface* function consisting of schematic pages 6 through 10. The third symbol is the *Low Voltage Lens Control* function consisting of schematic pages 11 through 16. The fourth symbol is the *High Voltage Control and Analog Readbacks* function consisting of schematic pages 17 and 18.

The first page schematic sheet shows the links and net type definitions. The status bits are connected to a status bus to show how each status bit from the various symbols are located within the status word. All of the chip selects, data buses, and address buses are connected at this level. The net types are defined on the right side of the page. The only net type definitions at this level involve the power signals on the board. These carry a net type of NET_PWR which is used by the layout tool to drive the thickness and spacing of power traces.

3.2 Page 2 of 18, Mass Adjustments

The main functions on this page are the Mass Axis DAC, the Mass gain and offset DACs, the AMU gain and offset DACs, and the summation amplifiers. Also, all of the support circuitry for these elements are on this page.

3.2.1 Mass Axis DAC

The Mass Axis DAC, U180, is a 16 bit self calibrating DAC that is used to step through the mass positions of the instrument. A 16 bit word is sent to the DAC through two writes; a high byte, and a low byte. To keep the DAC from changing during these writes, the high byte is written first which causes control logic in the FPGA to lower LDAC until the low byte is written. Once the low byte is written, LDAC is changed to a “1” which updates the internal output DAC. The DAC is calibrated by the MODE CONTROL word that toggles the ~DAC_CAL line. The DAC does a gain and offset calibration to guarantee a true 16 bit monotonic DAC with less than 1/4 LSB error (good to 17 bits). LED DS5 will light when the DAC needs calibration. This is sensed by the ~DACCAL_FLT line which feeds the STATUS1 register. The DAC is operated in a unipolar mode with a 0 to +10v output. The internal reference is used as the DAC reference which is fed by resistor R309. Resistors R465 and R466 are pullups. R464 biases the LED and R634 is a series resistor that allows testpoint, P52, to be used as a point to force a fault with external test equipment. U182 is used to buffer the reference voltage, however, the output is not used on the board, but was intended for future experiments. The equation that relates the output voltage to the 16 bit input word is as follows:

$$Vaxis = \frac{Daxis}{2^{16}} \bullet Vrefx \qquad [1]$$

Vrefx is the reference voltage of the DAC. *Daxis* is the digital 16 bit word (0 to 65535) written to the DAC. *Vaxis* is the voltage out of the DAC. When the actual values are used, the equation is simplified to:

$$Vaxis = \frac{Daxis}{65536} \bullet 10 \qquad [2]$$

The output voltage is buffered by U146 because of the limited current drive capability of the DAC. R564 is used to limit the current into the opamp in case the DAC output voltage changes faster than the opamp slew rate.

The main goal of the instrument was to have a mass range up to 3000 AMU. Using a 16 bit DAC gives a very nice relationship for a calibrated instrument with a range of 0 to 3276.75 AMU with a step size of 0.05 AMU. Therefore, the Mass DAC is designed into the electronics to give a single bit step of 0.05 AMU. The equation that relates the DAC to AMU is as follows:

$$DAC = 20 \bullet AMU \qquad [3]$$

The following table outlines the Mass Axis DAC relationship.

Table 2: Mass Axis DAC

Parameter	Address	Range	Resolution	Relationship
Mass Axis	164 high, 36 low byte	0 to 3276.75 AMU	0.05 AMU	DAC = 20 * AMU

The output of U146 pin 7 is buffered by U182 that sends an analog signal to the octopole board. The output of U146 pin 7 is sent as a reference for the Mass Gain and AMU Gain DACs. It is also sent to R493, which is a precise matched 10 Kohm resistor pair that is used to match the RF detected feedback signal with the mass set point. This resistor pair is connected to opamp U148 pin 2 that is used as an integrator in the RF control loop. The output of U148 pin 1 is designed to range from +10 volts to -10 volts that corresponds to 0 AMU and ~3200 AMU respectively. C307 and R71 make up the integrator compensation for the RF control loop. Components C298, C299, R507, and R508 are not loaded and were intended to be used as a "zero/pole" combination for the RF control loop. They were not needed, but were left on the board as no load components for future experiments.

3.2.2 Mass Gain and Mass Offset

The Mass Gain and Mass Offset DACs, U93, are used to calibrate the mass axis. Because of component tolerances in the electrical and mechanical design of the instrument, the Mass Axis DAC alone will not always provide an exact 0.05 AMU step. Therefore, the Mass Gain and Offset DACs calibrate the Mass position of the peaks to provide an exact 0.05 AMU step in the Mass DAC. This is very important for any Digital Signal Processing algorithm to make sure that any filtering or peak detection is applied equally across the mass range. In previous instrument designs, the gain and offsets were compensated in firmware. This caused many errors in peak shape and mass assignment simply because of rounding the mass assignment to a resolution of 0.05 AMU. The calibration in hardware eliminates all of these problems and eliminates the processing overhead of converting a DAC position to a mass assignment. Furthermore, by picking an appropriate ratio of gain and offset relative to Mass Axis control, the calibration can be done with a quick calculation as opposed to a search algorithm that tries to determine the proper gain and offset through an iterative approach. A complete derivation of the compensation method is provided in section 5.

The equation for the Mass Gain circuit is as follows:

$$Vmgain = -Vref \cdot \frac{Dmgain}{4096} \qquad [4]$$

Vmgain is the output voltage of U149 pin 1, *Vref* is the reference voltage of the DAC, U93(a), driven by the Mass Axis DAC, and *Dmgain* is the digital control word (0 to 4095) written to the DAC.

The equation for the Mass Offset circuit is as follows:

$$Vmoffset = -Vref \cdot \frac{Dmoffset}{4096} \qquad [5]$$

Vmoffset is the output voltage of U149 pin 7, *Vref* is a +5 volt reference voltage for DAC U93(b), and *Dmoffset* is the digital control word (0 to 4095) written to the DAC.

3.2.3 AMU Gain and AMU Offset

The AMU gain and AMU offset DAC are used to adjust the peak width. The AMU gain DAC is applied relative to the mass position having a stronger weighing function for higher masses. The AMU offset DAC is applied equally for all masses.

The equation for the AMU Gain circuit is as follows:

$$Vagain = -Vref \cdot \frac{Dagain}{4096} \qquad [6]$$

Vagain is the output voltage of U150 pin 1, *Vref* is the reference voltage of the DAC, U98(a), driven by the Mass Axis DAC, and *Dagain* is the digital control word (0 to 4095) written to the DAC.

The equation for the AMU Offset circuit is as follows:

$$Vaoffset = -Vref \cdot \frac{(Daoffset)}{4096} \qquad [7]$$

Vaoffset is the output voltage of U150 pin 7, *Vref* is a +5 volt reference voltage for DAC U98(b), and *Daoffset* is the digital control word (0 to 4095) written to the DAC

3.2.4 Mass Axis summation amplifier

U148 pins 1, 2, and 3 make up the Mass Axis summation amplifier. This opamp is configured as an integrator, but can be modeled as a summation amplifier to sum in all of the mass axis control voltages. The following diagram is the model of the opamp circuit.

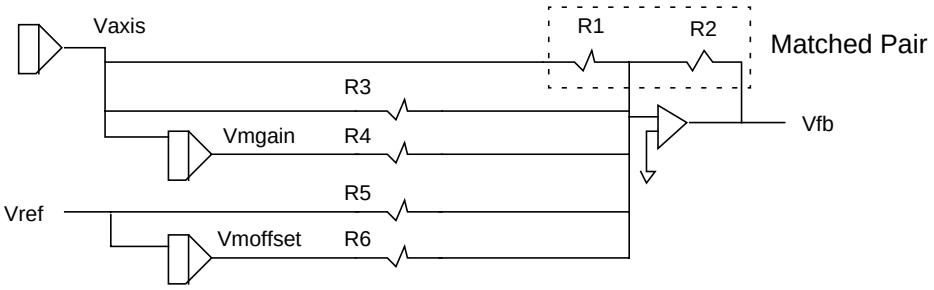

Figure 1. Mass Axis Summation Amplifier Model

The following is the output equation:

$$Vfb = -\frac{R2}{R1} \cdot Vaxis - \left(\frac{R2}{R3} \cdot Vaxis + \frac{R2}{R4} \cdot Vmgain\right) - \left(\frac{R2}{R5} \cdot Vref + \frac{R2}{R6} \cdot Vmoffset\right)$$

The goal of this equation is to generate a relationship of *Vmgain* and *Vmoffset* such that the digital control words applied are in units of AMU. Furthermore, the gain and offset terms need to be bipolar. In the SPRITE design, R1=R2, R3=2R4, and R5=2R6. The equation simplifies to:

$$Vfb = -Vaxis - \left(\frac{R2}{R4} \cdot \left(\frac{1}{2} \cdot Vaxis + Vmgain\right)\right) - \left(\frac{R2}{R5} \cdot \left(\frac{1}{2} \cdot Vref + Vmoffset\right)\right) \qquad [8]$$

Substituting Equations [4] and [5] into [8] gives:

$$Vfb = -Vaxis - \left(\frac{R2}{R4} \cdot \left(\frac{1}{2} \cdot Vaxis - Vaxis \cdot \frac{Dmgain}{4096}\right)\right) - \left(\frac{R2}{R5} \cdot \left(\frac{1}{2} \cdot Vref - Vref \cdot \frac{Dmoffset}{4096}\right)\right)$$

This is reduced to:

$$Vfb = -Vaxis - \left(\frac{R2}{R4} \cdot Vaxis \cdot \left(\frac{1}{2} - \frac{Dmgain}{4096}\right)\right) - \left(\frac{R2}{R5} \cdot Vref \cdot \left(\frac{1}{2} - \frac{Dmoffset}{4096}\right)\right)$$

Now substitute equation [2] and Vref=+5v to get:

$$Vfb = -\left(\frac{(Daxis)}{65536}\cdot 10\right) - \left(\frac{R2}{R4}\cdot\frac{(Daxis)}{65536}\cdot 10\cdot\left(\frac{1}{2} - \frac{Dmgain}{4096}\right)\right) - \left(\frac{R2}{R5}\cdot 5\cdot\left(\frac{1}{2} - \frac{Dmoffset}{4096}\right)\right) \qquad [9]$$

Axis DAC — Gain DAC — Offset DAC

From this equation, one can see the three components of summation and how they affect the feedback voltage, *Vfb*. Now, the values of R4 and R5 must be properly chosen to give some meaning to the gain and offset terms. The value of R2 is 10 Kohm, which is matched with R1 from the figure above. R493 of the schematic is the 10k/10k matched pair. Starting with the offset term of equation [9], R5 is chosen such that one count of the Mass Offset DAC produces 0.002 AMU, or 1/25 of one count of the Mass Axis DAC.

$$\frac{1}{25}\cdot\left(\frac{(1)}{65536}\cdot 10\right) = \left(\frac{R2}{R5}\cdot 5\cdot\frac{(1)}{4096}\right)$$

Solving for R5:

$$R5 = \left(\frac{65536}{4096}\right)\cdot\frac{(25\cdot 5)}{(10)}\cdot R2 = 200\cdot R2$$

Therefore,

$$R5 = 2Mohm$$

Now, using the gain term of equation [9], R4 is chosen such that one count of *Dmgain* is equal to 0.05 AMU (1 count of *Daxis*) at 3276.8 AMU. The Mass Axis DAC only goes to 3275.75 AMU with a count of 65535. Therefore, a count of 65536 will be used in the equation to get the proper relationship.

$$\frac{(1)}{65536}\cdot 10 = \frac{R2}{R4}\cdot\left(\frac{65536}{65536}\right)\cdot 10\cdot\frac{(1)}{4096}$$

Solving for R4:

$$R4 = \left(\frac{65536}{4096}\right)\cdot R2 = 16\cdot R2$$

Therefore,

$$R4 = 160Kohm$$

Rewriting equation [9]:

R. ROUSHALL DRAWN BY	07/29/97	**Analyzer PCA Assembly Theory of Operation** TITLE	HEWLETT PACKARD
R. ROUSHALL ENGINEER	07/29/97		
B. CAPRILES RELEASE TO PROD.	01/15/98		G1946-60001 PART NUMBER
SUPERSEDES DWG.	CURRENT REV B	PAGE 9 OF 45	**A-G1946-60001-5**

$$Vfb = -\left(\frac{(Daxis)}{65536}\cdot 10\right)-\left(\frac{1}{16}\cdot\frac{(Daxis)}{65536}\cdot 10\cdot\left(\frac{1}{2}-\frac{Dmgain}{4096}\right)\right)-\left(\frac{1}{200}\cdot 5\cdot\left(\frac{1}{2}-\frac{Dmoffset}{4096}\right)\right) \quad [10]$$

Using the values of 0 to 4095 for *Dmgain* and *Dmoffset*, the following table is derived.

Table 3: Mass Gain & Offset

Parameter	Address	Range	Resolution	Relationship
Mass Offset	29	-4.096 to +4.094 AMU	0.002 AMU	DAC = 2048 + 500 * AMU
Mass Gain	38	-102.4 to +102.35 AMU @ 3276.8 AMU	0.05 AMU @ 3276.8 AMU	DAC = 2048 + 20 * AMU

3.2.5 AMU Summation Amplifier

U148 pins 5, 6, and 7 make up the AMU summation amplifier that drives the U+/U- circuitry. The model for the summation amplifier is identical to the model of the Mass Axis shown in Figure 1. However, instead of just the AMU gain and offsets driving the summation amplifier, the Mass gain and offsets also drive the summation point. This is done so that the peak widths do not change when Mass gain and offset are applied. The Mass gain and offset terms have to sum into both the RF and DC control loops in order to keep the RF/DC ratio constant. The following model is used to represent the AMU summation amplifier.

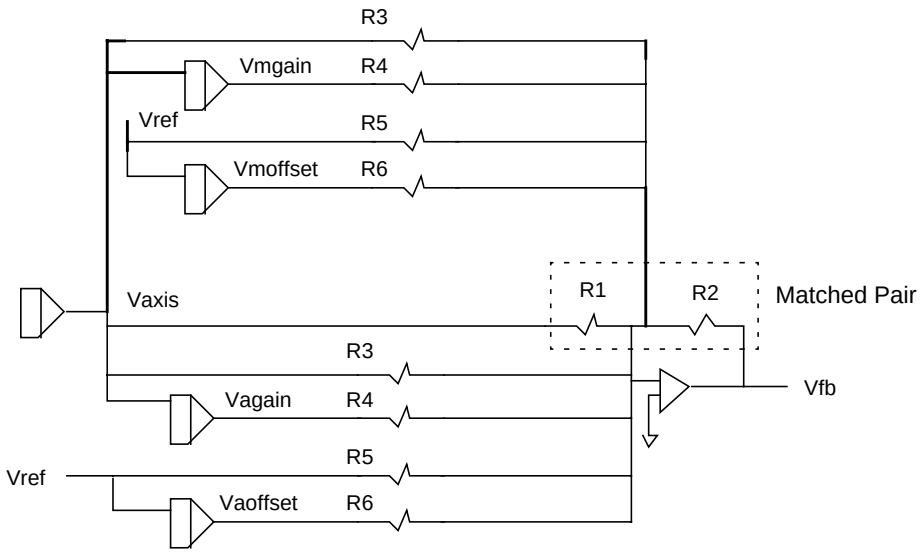

Figure 2: AMU Summation Amplifier Model

The analysis of the AMU summation model is identical to the Mass Axis summation model. The resistor values are the same to give the same weighting to the AMU gain and offset as the Mass gain and offset. The model, however, can be simplified. The resistors R3 of the top and bottom stages of the AMU model are in parallel, as are the resistors R5. Since the weightings are the same, the relationships are the same. The AMU offset term has a resolution of 0.002 AMU peak width and the AMU gain term has a resolution of 0.05 AMU peak width at 3276.8 AMU. For small changes in peak width, these relationships hold true. However, for large changes

in peak width, the relationships are not quite linear. The peak width change has a second order affect that starts to dominate the peak width adjustment. Furthermore, the peak width adjustments are not linear across the mass range. The resolution of the adjustments at higher mass are less affective than at lower mass. Because of these second order effects, the units of AMU gain and offset were kept in the units of DAC counts in bipolar format. The following table outlines the AMU gain and offset relationships.

Table 4: AMU Gain & Offset

Parameter	Address	Range	Resolution	Relationship
AMU Offset	21	-2047 to +2048 #	1 #	DAC = 2048 - #
AMU Gain	37	-2047 to +2048 #	1 #	DAC = 2048 - #

3.2.6 Diode Compensation Summation Amplifier

U146 pins 1, 2, and 3 along with resistors R318, R319, and R630 make up a diode compensation summation amplifier. The goal of this circuit is to create a buffered output voltage that is proportional to mass position. The output feeds a diode circuit on schematic sheet 4. R318 and R319 create a "-1" amplifier to create an output voltage of 0 to -10 volts. R630 provides a little bias voltage to keep the diode from reverse biasing. The bias voltage is equal to about 350 AMU. This could be adjusted much lower to maybe 10 AMU.

3.3 Page 3 of 18, U+/U- Amplifiers

The components on sheet 2 make up two amplifier stages for driving the U+/U- DC voltages. Both amplifier stages are unipolar to provide the complementary voltages. The components are divided into three functional areas; 1) the low voltage stage, 2) the high voltage stage, and 3) the output coupling.

3.3.1 Low Voltage Stage

The DC drive signal from the AMU summation amplifier comes in on the signal named DC_DRIVE_LVL. This signal is summed into opamp U145 in two points; pin 2 and pin 5. Another signal called QUAD_OFFSET also feeds the amplifier stage. Its goal is to provide a fixed offset on the U+/U- outputs. Resistors R1 and R2 are high voltage precision resistors that feedback the high voltage outputs for the low voltage stage. R61 sets the gain of the amplifier. The following is a model of the U+/U- amplifier.

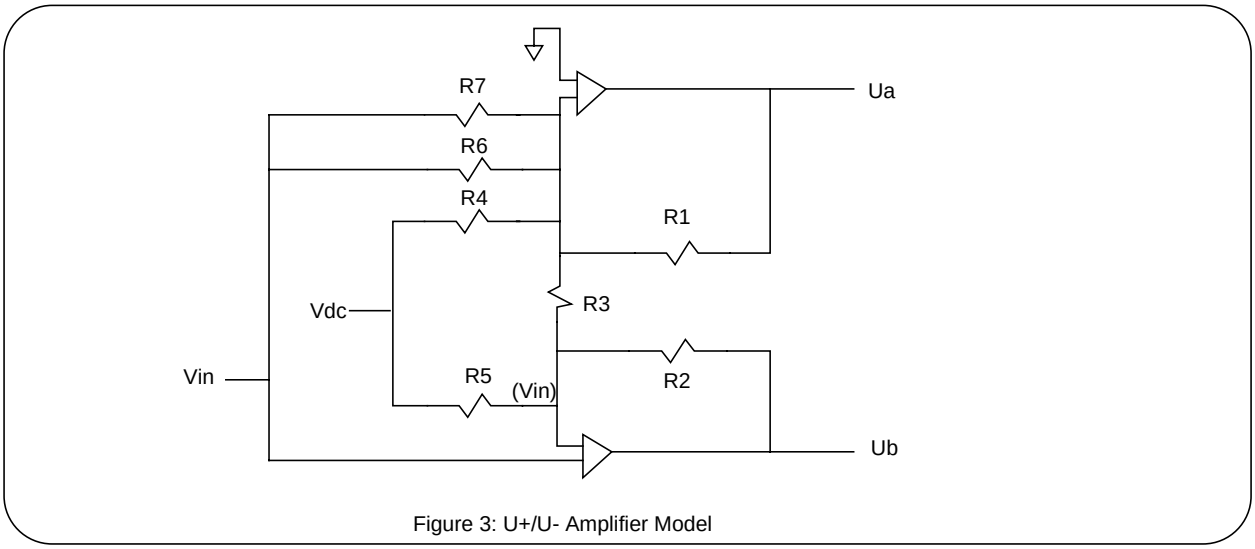

Figure 3: U+/U- Amplifier Model

The amplifiers in this model are not just opamps, but they include the transistor stages to get out high voltage. Those details are left out of the model and it can be assumed that the opamps in the model are ideal opamps. The following are the current summation equations for *Ua* and *Ub*.

$$\frac{Ua}{R1} + \frac{Vin}{R7} + \frac{Vin}{R6} + \frac{Vin}{R3} + \frac{Vdc}{R4} = 0$$

$$\frac{(Ub - Vin)}{R2} + \frac{(Vdc - Vin)}{R5} + \frac{(0 - Vin)}{R3} = 0$$

Solving for *Ua* and *Ub* gives the following

$$Ua = -Vin \cdot \left(\frac{R1}{R7} + \frac{R1}{R3} + \frac{R1}{R6}\right) - \left(Vdc \cdot \frac{R1}{R4}\right) \quad [11]$$

$$Ub = Vin \cdot \left(1 + \frac{R2}{R3} + \frac{R2}{R5}\right) - \left(Vdc \cdot \frac{R2}{R5}\right) \quad [12]$$

Substitute R1=R2=R7 and R4=R5=R6

$$Ua = -Vin \cdot \left(1 + \frac{R1}{R3} + \frac{R1}{R4}\right) - \left(Vdc \cdot \frac{R1}{R4}\right) \quad [13]$$

$$Ub = Vin \cdot \left(1 + \frac{R1}{R3} + \frac{R1}{R4}\right) - \left(Vdc \cdot \frac{R1}{R4}\right) \quad [14]$$

These two equations are now very similar. The *Vin* term creates equal and opposite voltages. The *Vdc* term creates a common voltage on the outputs. The goal now is to match the Ua and Ub equations to the Mathieu equation for the DC voltage on a quadrupole with sinusoidal RF drive operated in the first stability region.

$$Udc = 1.21 \cdot N \cdot f^2 \cdot R0^2$$

N Is The AMU setting, *f* is the RF frequency in MHz, and *R0* is the radius of the quad in inches. The equation can be rewritten in the form,

$$Udc = 1.21 \cdot N \cdot 10^{-12} \cdot fo^2 \cdot R0^2 \quad [15]$$

For the SPRITE instrument, *N* is 3276.8 AMU for 10 volts of input voltage, *fo* is nominally 1.0 Mhz, and *R0* is 0.4445 [in]. Substituting these values into the equation, you get;

$$Udc = 783.3915$$

Therefore, when *Vin* = 10 volts and *Vdc* = 0 volts from figure 3,

$$Ua = -10 \cdot \left(1 + \frac{R1}{R3} + \frac{R1}{R4}\right) = -783.3915$$

$$Ub = 10 \cdot \left(1 + \frac{R1}{R3} + \frac{R1}{R4}\right) = 783.3915$$

From here, the resistors are chosen that best fit the voltage gain and offset terms of the equations.

$$R1 = 2.0Mohm$$

$$R3 = 29.4Kohm$$

$$R4 = 200Kohm$$

Using these values, equations [13] and [14] simplify to;

$$Ua = -(79.0272 \cdot Vin) - (10 \cdot Vdc) \qquad [16]$$

$$Ub = (79.0272 \cdot Vin) - (10 \cdot Vdc) \qquad [17]$$

All of the resistor values listed above were used for resistors R1, R2, R61, R64, R65, R66, R88, and R90 on the schematic sheet. These resistors make up all of the gain and offset functions for the U+/U- amplifiers.

There are a few other components on the low voltage amplifier stage. R462 and C306 help slew rate and current limit the input of opamp U145. Without the components, the opamps would go non-linear for a large step input and they would take longer to recover. These components actually speed up the step response of the U+/U- stage. R544, C135, R543, and C134 are compensation networks for the opamps. They help stabilize the low voltage opamp stage and were determined experimentally from small and large signal responses from the input voltage. Compensation networks C296, R505, R556 and C297, R506, R555 are pole/zero compensations for the high voltage stage. They provide a ZERO at 6.84 Khz and a POLE at 89.7 Khz. This compensation is used to match the performance of the high voltage stage.

3.3.2 High Voltage Stage

The high voltage stage consists of the input bias transistors, the optocouplers, and the output transistor stacks. The input bias transistors take the output of the compensation networks and drive the ends of the transistor stacks. One end is connected through the input of the optocoupler. The other end is connected to the bottom stage of the transistor stack. The input bias transistors are standard NPN and PNP transistors. The diodes CR29 and CR30 along with resistors R82, R74, and R75 bias the input transistors. Diodes CR32 and CR33 help remove the diode drops of the input transistors. The goal is to provide a smooth transition from turning off the optocoupler to turning on the bottom transistor of the transistor stack and vice-versa. The transistor stacks are high voltage transistors that are biased by the resistor stack to evenly divide the voltage across the transistors. The rails are set to approximately 812 volts. When the U+/U- are commanded to 0 AMU (or 3000+ AMU) the rail voltage must evenly divide across the “off” transistors. This means that the “off” transistors must be able to handle 270 volts (812/3) from collector to emitter. There are two high voltage diodes, CR51 and CR52, that provide extra base drive to the high voltage stack to help the output voltages reach 0 AMU. Without the diodes, the transistors that pull to the +/- 15 volt rails may saturate causing a limit in the output voltage. The output of the transistor stacks then feeds the output coupling stage.

3.3.3 Output Coupling Stage

The output coupling stage consists of a filter, a relay switch, and a 1Mhz choke. Looking at the U+ output, components R325, R326, C38 and C40 make up the filter. These components filter in both directions. The capacitors are stacked to divide the output voltage across them. The relays K1, K2, K3, and K4 are used to switch quad polarity. Since the U+/U- amplifiers are unipolar drivers, the relays switch the output voltages on connector P4. The control inputs to the relays are high current drive NPN transistors, Q79 and Q80, that act as switches. The control inputs, QD_PLRTY_A and QD_PLRTY_B, are designed as "break-then-make" signals to minimize current pulses. The software is also designed to set the Mass position to 0 AMU before switching polarity. The transistors are also protected by flyback diodes CR41 and CR42. Components L11, C291, C292 and L12, C293, C294 are 1Mhz chokes. Their goal is to minimize any 1Mhz ripple from getting into the sensitive amplifiers. If any ripple gets through, the amplifiers exhibit a non-linearity in their gain function. This causes non-linear peak widths.

3.4 Page 4 of 18, RF Detect

The components on this page make up the RF Detection circuit. The main goal of this circuit is to sample the peak RF voltage on the quad that is used by the RF control loop The circuit must be precise and stable in order to have good peak stability. There are three sections on this sheet; 1) the RF detect circuit, 2) the diode compensation circuit, and 3) the heater circuit.

3.4.1 Detect Circuit

The Detect circuit is designed to sample both phases of the nominal 1Mhz RF voltage and generate a voltage that is proportional to the peak voltage on the quad. The sampling and rectifying of the 1Mhz signal is performed by assembly G1946-60005. The rectified signal is brought onto the Analyzer board through connector J3 pin 7. This signal is a current that is proportional to the peak voltage on the quad. L13, C301, and R304 filter the signal to get an average DC current. U147 is the opamp that converts the current to a voltage. Q109 buffers the opamp and R490 and C309 stabilize the opamp. The resistors R86 and R87 set the gain of the detect circuit such that 0 to 3276.8 AMU corresponds to 0 to -10 volts. The output voltage on net MASS_FBPT is sent to sheet 1 and summed into the Mass Axis summing amplifier. The two resistors, R86 and R87, are the most precise resistors on the sheet. Two resistors were chosen to minimize self heating of the components. The nominal resistance is 476.5 Ohms.

As mentioned in section 3.2.1, the Mass Axis DAC is designed to step 0.05 AMU with a range of 3276.75 AMU. To make this happen, the Detect circuit must match this requirement. The basis of the Detect circuit is the Mathieu equation for RF voltage on a quadrupole with sinusoidal drive operated in the first stability region.

$$Vpeak = 7.22 \cdot N \cdot f^2 \cdot R0^2$$

The equation can be rewritten in the form;

$$Vpeak = 7.22 \cdot N \cdot 10^{-12} \cdot fo^2 \cdot R0^2 \qquad [17]$$

Vpeak is the peak voltage on the quad, *N* is the AMU setting, *fo* is the frequency of the RF signal in Hz, and *R0* is the radius of the quad in inches. The Mathieu equation used a frequency, *f*, that was in units of Mhz. Rewritting the equation in units of Hz makes it more usable in future discussions. For the SPRITE instrument, *N* is 3276.8 AMU for a detected voltage of -10 volts, *f*o is nominally 1 Mhz, and *R0* is 0.4445 [in]. Figure 4 is a model of a sampling and detect circuit that represents the circuit in SPRITE for measuring the peak voltage.

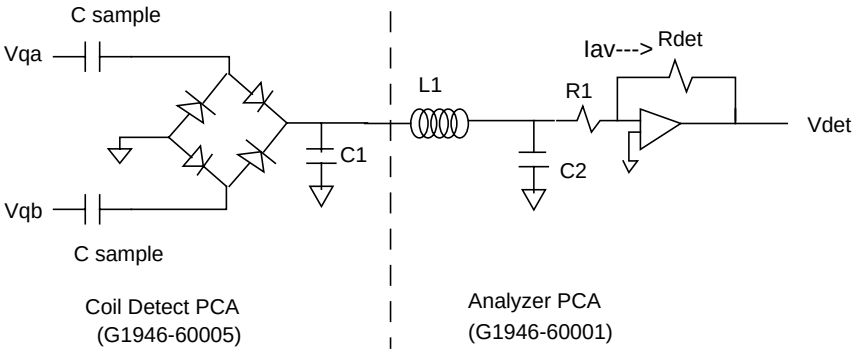

Figure 4: RF Detect Circuit Model

Using figure 4, the goal is to determine the value of *Rdet* such that the voltages, *Vqa* and *Vqb*, meet the Mathieu relationship of equation [17]. The left half of the detect circuitry exists on the Coil Detect PCA. The sampling capacitor assembly creates the two capacitors that sample the voltages. The diodes rectify the current out of the sampling capacitors and send it to the detect circuit on the Analyzer board. The opamp gains the signal by *Rdet* to create an average voltage, *Vdet*, that is proportional to *Vqa* and *Vqb*.

The generic equation for average current is:

$$Iav = \frac{1}{T}\int_0^T i\,dt$$

Since the signal is sinusoidal and rectified, the equation is simplified.

$$Iav = \frac{1}{\frac{1}{2}\cdot T}\int_{-\frac{T}{4}}^{\frac{T}{4}} Ipeak\cos\frac{2\pi t}{T}\,dt$$

This integral is evaluated to;

$$Iav = \frac{2}{\pi}Ipeak$$

Since *Ipeak* is a function of the quad voltage and sampling capacitor, the equation becomes:

$$Iav = \frac{2}{\pi}(Vpeak\omega C) \qquad [18]$$

Solving for the voltage out of the detect circuit;

$$Vdet = -Iav\cdot Rdet$$

Therefore,

$$Rdet = -\frac{Vdet}{Iav} \qquad [19]$$

Substituting equations [17] and [18] into [19] gives,

$$Rdet = -\frac{Vdet}{\left(\frac{2}{\pi} \cdot 7.22 \cdot N \cdot 10^{-12} \cdot fo^2 \cdot R0^2 \cdot \omega \cdot C\right)}$$

Simplified,

$$Rdet = -\frac{Vdet}{4 \cdot 7.22 \cdot N \cdot 10^{-12} \cdot fo^3 \cdot R0^2 \cdot C} \qquad [20]$$

For the SPRITE design, *Vdet* = -10 volts at *N* = 3276.8, *R0* = 0.4445 [in], *fo* = 1 Mhz, and *C* = 1.1 pF. Substituting these values into the equation,

$$Rdet = 486 \text{ Ohms}$$

The value that is used on the board is 476.5 Ohms. This was determined experimentally and from components already available. The value of the capacitance of the detect circuit was determined experimentally and may not be exactly the value of the sampling capacitor assembly, however, it is accurate enough for determining the resistance needed in the detect circuit.

3.4.2 Diode Compensation Circuit

The diode compensation circuit consists of U147, R84, R85, R306, R307, R83, C138, and R235. The main goal of the circuit is to take out the affects of the rectifying bridge and resistor R1 of figure 4. These components cause an error in detecting the voltage on the quad. They also have temperature affects that can cause mass position and peak width errors. The following diagram is the model of the compensation circuit.

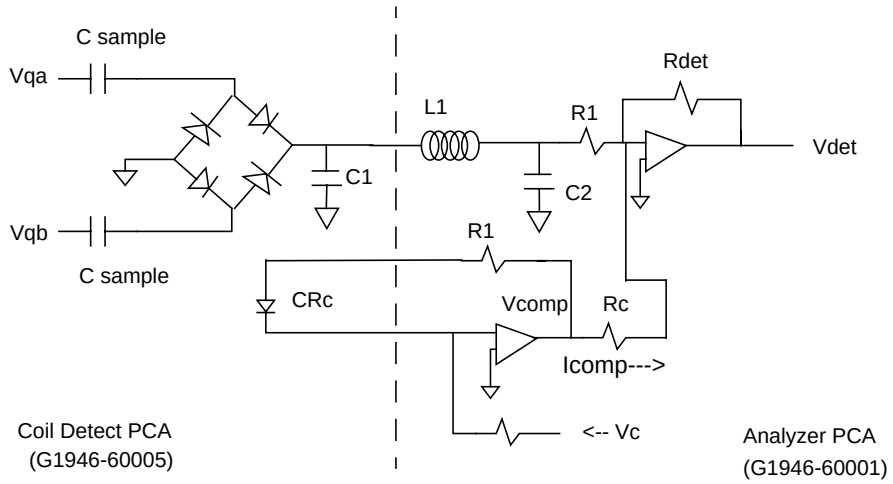

Figure 5: Detect Circuit with Diode Compensation

The compensation diode, *CRc*, is thermally coupled to the rectifying diodes to keep the diode Tc effects the same. Voltage, *Vc*, drives the compensation circuit to generate a current through the diode, *CRc*, that is proportional to the current in the rectifying diodes. Resistor *Rc* is selected such that the compensation circuit subtracts out the voltages generated by the rectifying diodes and resistor *R1*. The goal is to add current from the compensation circuit that is equivalent to the amount of current lost from the theoretical analysis of the sampling capacitors due to the rectifying bridge and resistor *R1*.

The following simplified model is used to describe the relationship of the components in the detect circuit to the theoretical

model.

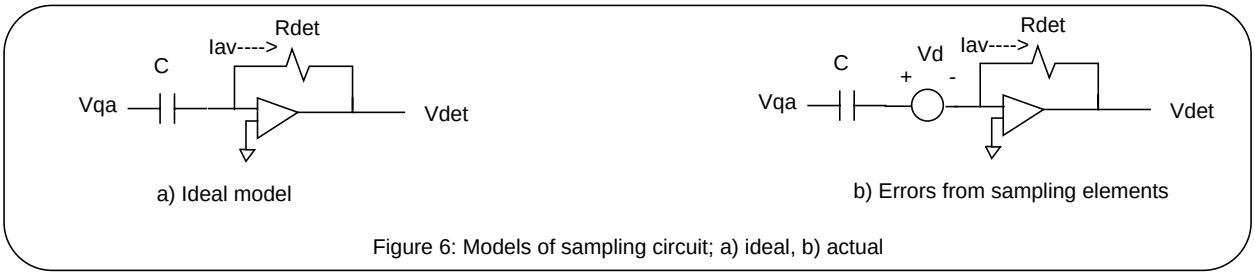

Figure 6: Models of sampling circuit; a) ideal, b) actual

Writing the equations for the models;

{ model a. } $$Iav = Vqa \cdot \omega \cdot C$$

{ model b. } $$Iav = \frac{Vqa - Vd}{1/\omega \cdot C} = (Vqa \cdot \omega \cdot C) - (Vd \cdot \omega \cdot C)$$

where,

$$Icomp = Vd \cdot \omega \cdot C \qquad [21]$$

The error in current from the actual implementation is from the voltage, *Vd*, times the impedance of the sampling capacitor. The compensation circuit generates the voltage, *Vd*, by using the same diode and resistor in the detect circuit such that a compensation current (*Icomp*) is generated that is equal to the error term of the previous equation. Since the current in any one of the rectifying diodes only occurs every other cycle, the current needed in the compensation diode is only half the average current in the rectifying circuit. This keeps the power about the same through the devices which is key to matching the thermal properties. Furthermore, there are 2 diodes per package, so both diodes in the package are used in the compensation circuit.

Using figure 5 as the model, the voltage, *Vd*, of figure 6 b) is:

$$Vd = Vdiode + (Iav \cdot R1)$$

The voltage from the diode compensation circuit (figure 5) on U147 pin 7 is:

$$Vcomp = (2 \cdot Vdiode) + (Iav \cdot 2R1) = 2 \cdot (Vdiode + (Iav \cdot R1)) = 2 \cdot Vd \qquad [22]$$

Since the voltage developed is twice the voltage lost in the detection circuit, the resistor, *Rc*, of figure 5 is twice the impedance of the capacitor in the detection circuit. Using equation [21] and [22],

$$Rc = \frac{Vcomp}{Icomp} = \frac{(2 \cdot Vd)}{Vd \cdot \omega \cdot C} = \frac{2}{\omega \cdot C}$$

For SPRITE, the frequency is 1 Mhz and the sampling capacitor is 1.1 pF. Therefore,

$$Rc = 289Kohm$$

On the schematic sheet, the resistance is split between R235 and R83. This allowed for a filter capacitor, C138, that was needed to reject any RF voltage coming in from the compensation diodes. The diodes reside inside the coil box assembly where there is a tremendous amount of magnetic field.

3.4.3 Heater Circuit

There are four zones in the heater circuit labelled zone A through zone D. Four zones where chosen because of the amount of power needed to heat the metal can that shields all of the sensitive circuits on the Analyzer board. Each zone operates exactly the

same.

The first part of the heater design is the bridge network setup by resistors R615, R617, R618, R482, R484, R585, R587, and RT1-RT4. The bridge network is biased between ACOM and -15V. ACOM is not only the ground of the circuit, but it is the copper area that heats the metal can. Figure 7 is a simplified diagram of the bridge circuit.

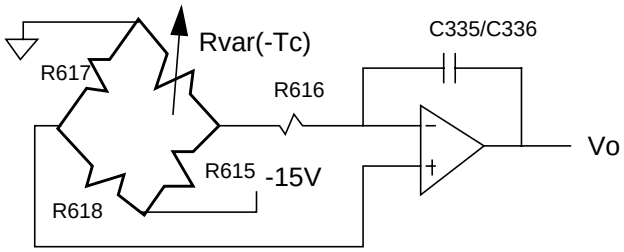

Figure 7. Bridge Circuit

The bridge circuit is biased at -7.5v by resistors R617 and R618. This bias is half way between the bias of the opamps, U177 & U163, and the heaters. This allows for operation of the heater design over the largest range. *Rvar* in Figure 7 is a combination of RT1-RT4 and R482, R484, R585, and R587. When *Rvar* equals R615, then the integrator stops integrating and a balance point is met. As the board heats up, *Rvar* becomes smaller which makes *Vo* less. Each RT resistor is weighted with a series resistor (for example, RT1 with R484) to provide a "gain" of the temperature resistive device. The time constant of the integrator is very long because of the thermal time constant of the heaters and the temperature sensors.

The voltage out of the integrator is sent as a set point to the four heater zones. Zone A takes the voltage directly and the other three zones buffer the voltage with the spare opamps in U177 and U163. Using heater zone A as an example, the heater is a biased power transistor, Q112, that simply generates heat by dissipating power out the collector. The collector of the transistor is tied to ACOM which is common to the metal can. The set point voltage is first dropped by a zener diode, CR44. This helps keep the integrator near the center of the bias voltage during normal operation. Following the zener diode are two resistors. The first resistor, R590 provides some base resistance to the transistor. The second resistor, R588 is used to guarantee that the power transistor is off when the integrator drives to a lower voltage (pull down resistor). The resistors R622, R581, and R582 are emitter resistors. They keep the transistor biased properly and also set the "heat" gain of the transistor. The smaller the resistance, the higher the gain of the transistor. Three resistors used to help dissipate the current through the emitter. The other zones operate exactly the same.

3.4.4 Miscellaneous

There are a few miscellaneous items on this page. The resistor, R503, is intended to change the gain of the detect circuit. This would be needed if the instrument did not have enough Mass Gain to compensate the peak positions. By using jumper P41, the gain will change that will shift the Mass gain of the instrument. This is not used in the SPRITE instrument since the tolerances of the instrument keep the gain within specification of the Mass Gain adjustment range.

The components at the top of the page that sum into the detect opamp, are used when a shutdown condition exists. During a shutdown, the transistor, Q114, turns on and sums current into the detect opamp. This will act as though a fair amount of RF voltage exists on the quad. This will force the error amp on sheet 2 to completely shut off the RF signal.

3.5 Page 5 of 18, U+/U- Supplies

This schematic sheet contains the DC/DC power supplies for the U+/U- rails and the IRIS/FRAGMENTOR rails. U168 generates the negative rail for U- and U170 generates the positive rail for U+. These supplies are 1000v DC/DC converters. Each output is filtered to help minimize any ripple from the DC/DC converters. U169 generates the negative rail and U171 generates the positive rail for the IRIS/FRAGMETOR lenses. U175 and U176 are +12 volt regulators that supply power for the converters. U152 buffers the voltage divider stages that set up the control voltage for the converters. The U+/U- supplies need a control voltage of 4.06 volts to generate an output of ~812 volts. The IRIS/FRAGMENTOR supplies need a control voltage of 4.53 volts to generate an output voltage of ~453 volts.

3.6 Page 6 of 18, Bus Connect

This schematic sheet has the MSE bus connection components. The 96 pin connector, J2, connects to the bus board in the bottom of the SPRITE tub. The components U131 and U167 gate the read and write strobes together and they delay the rising edge of the ~MS_WR signal so that the analyzer data bus, AN_DB(15:0), is driven some time after the rising edge of the write strobe. This keeps the data on the bus long enough to allow for chip select logic delay times in the FPGA. U142 and U143 buffer the data bus between the bus board and the Analyzer board.

3.7 Page 7 of 18, Decode

This schematic sheet brings together most of the interfaces to the FPGA. The main functions on this board are the source interlocks, the status readbacks, the display board interface, and the multiple chip select and control lines from the FPGA.

The source interlocks are implemented with the components in the top left of the schematic. There are three interlocks; 1) Needle ID, 2) high voltage Source Interlock, and 3) the Source ID. Each interlock operates the same. Using the Needle ID as an example, the connector P33 provides a contact closure signal from an external device such as a magnetic relay. When the relay is open, P33 pin 2 has +5v with a series resistor of 464 Ohms, R537. The other pin has a pull down, R468, that pulls the line to ~0 volts. The FPGA reads this signal as a logic low. When the relay closes, pin 1 and pin 2 are shorted together which changes the logic level to high (~3 volts). Therefore, the FPGA can sense when any of the interlocks are open or closed. The transorbs, CR45, CR46 and CR47, protect the lines from ESD events. From a safety point of view, the design is made to have a high logic state when the relay is closed. This is considered a “safe” condition. Should the external cable ever short to the chassis or the magnetic relay fails, this condition is sensed as a problem. The logic lines of all three interlocks are fed to the FPGA where they are decoded for fault conditions.

The status readbacks consist of U165 and U130. U165 is read during a status 2 read and is a means to read the interlock conditions directly. U130 takes the internal shutdown status bit and drives an external shutdown line that is sensed by other boards plugged in the bus board.

The display board interface is a buffer, U166, that drives three control lines out J4. These control lines turn on and off LEDs on the display board. The display board is also powered from J4 with +5V and ground. There are a set of capacitors on each line to minimize RFI problems with the cable to the display board. The cable leaves the EMI tub.

The center of the schematic page is a hierarchal symbol for the FPGA. This device performs all of the decoding for the devices on the board as well as other control functions. All of the chip selects are brought out on the right side of the schematic. Some of the functions have additional logic. The LDAC signal is used to open and close a latch on the Mass Axis DAC. The latch is closed quickly during a high byte write. This keeps the Mass Axis DAC from updating until the low byte is written. When the low byte is written, the LDAC signal is delayed slightly to guarantee the setup time of the DAC. U167, pins 8/9 and 10/11, buffers the controls lines that change the quad polarity. The FPGA does not have much drive capability, so the buffers add better drive to the transistors that switch the relays for U+/U-. U131 gates the Power On signal and the Shutdown signal to create a global shutdown for the board.

3.8 Page 8 of 18, RF Modulator

The functions on this sheet include the RF modulator, the drive level, and the RF fault circuitry. The RF drive signal comes from the error amp on sheet 2 with the net name RF_DRIVE_LVL. This signal feeds two functions; the drive level circuit, and the Direct Digital Synthesis (DDS) and compensation circuit. U174 with its resistors and capacitors make up the drive level circuit. The circuit puts out a 0 to +10 volt signal that is proportional to the amount of RF drive. The output is divided by R561 and R562 to generate a 0 to +5 volt signal, RFDRV_LVL, for the muxed ADC of sheet 18. The capacitors C353 and C305 delay the response of the drive circuit to keep it from responding from overshoot in the error amp. If a full range mass jump occurs, the error amp will rail for a small amount of time until the RF loop is back in control. During this time, it is important to not trip an RF fault. The RF fault circuit consists of U125 and the surrounding components. The resistors R300, R301, and R299 form a resistor divider to create a +10 volt signal on the positive lead of the comparator. R399 and CR50 keep the negative lead from going below the voltage rail of the part. CR50 also provides a little bit of margin on the drive signal so that the modulator can run up to 100% without tripping a fault. The output of U125 feeds the FPGA to generate a status 1 fault.

The DDS circuit is used to generate the nominal 1 Mhz RF signal and modulate the incoming level signal. The level signal first passes through the compensation circuit R557, R509, C300 and C337. This circuit puts in a ZERO at 3.7 Khz and a POLE at 92 Khz. This is used to compensate for the RF loop characteristics that are dominated by a POLE from the tank circuit. The tank circuit is the inductance of the high Q coils and the capacitance of the quad. Because of the high Q of the tank, a POLE exists at approximately 3.7 Khz. The compensation network cancels the POLE and increases the bandwidth of the RF control loop to greater than 60 Khz. This bandwidth is needed to increase SCAN speed and stabilize the peaks. Resistor R639 is used to bias the DDS input level to allow for

a +10v to -10v range on the incoming RF drive level.

U181 is the DDS chip that performs the signal generation and modulation. U126 provides a base clock of 20 Mhz for the DDS chip. R375 and C151 control the enable signal for the crystal keeping the crystal disabled until power is fully applied. R317 is used to dampen the clock output to control RFI. Resistor network R280 pulls up the data lines on the DDS chip to provide a high level input signal that is better than standard TTL. Pin 4 of the DDS chip is used as the input modulation control. This pin is a voltage reference of 1.25 volts and modulates the output by controlling the amount of current drawn from the reference. Pins 1 and 2 are complementary current drive signals that are used to drive a preamp circuit that eventually drives the RF Power Amplifier. R545 through R548 are the load resistors for the current drive signals to convert the current to voltage. C312 and C313 are used to smooth the output of the current drive signals. The current drive signals are direct outputs of the internal DAC of the DDS chip that need smoothing to create a sinusoidal RF signal. U164 is a high speed, high drive opamp to drive the RFPA. The resistors R627, R628, R558, and R559 are used to gain up the differential signal from the DDS, and resistors R549 and R550 are used to create a 50 Ohm output impedance.

The digital control of the DDS is accomplished by writing to the 8 bit data bus of the chip. The functions used in the chip include the FREQ0 register and the command register. None of the digital modulation registers are used in the chip. The FREQ0 register is loaded with a 32 bit value that sets the output frequency. The frequency is generated by a Numerically Controlled Oscillator (NCO) that is driven by the FREQ0 register. The relationship of the output frequency with respect to the FREQ0 register is as follows:

$$Fout = \frac{(FREQ0)}{2^{32}} \cdot Fclock$$

Fclock is the base clock of 20 Mhz, *FREQ0* is the 32 bit value of the phase register, and *Fout* is the frequency of the output drive signal. The range of FREQ0 is 0 to 2^{32}-1. This allows for a frequency range of DC to almost 20 Mhz. The resolution is 0.0047 Hz. For our application, FREQ0 is set to nominally 1 Mhz with a typical range of +/- 10 Khz.

Table 5: DDS Control

Parameter	Address	Range	Resolution	Relationship
Quad Frequency	144 data, 145 control	DC to 20 Mhz	4.7 millihertz	Count = 2^32 * (Freq[Khz]/20000)

For a complete description of the DDS chip, see the data sheet for an Analog Devices AD7008.

3.8.1 Frequency adjustment range

There are a few ramifications in adjusting the frequency. The main goal of the DDS circuit is to give us the ability to find the resonant frequency of the tank circuit. This “automated” method eliminated the slugs in the coils that are used in previous designs. As described in section 3.2 and 3.3, the Mass Axis calibration and AMU calibration are functions of the frequency on the quad. The resistance values of the RF Detect and U+/U- circuits were determined using a nominal frequency of 1.0 Mhz. If this frequency changes, then the mass position and peak width will change. This will require a change in Mass Gain and AMU Gain since these two parameters are functions of frequency. The Mass Offset and AMU Offset are not functions of frequency and would therefore not need changing when the frequency changes.

Rewriting the equation for RF Detect voltage from equation [20];

$$Vdet = -4 \cdot 7.22 \cdot N \cdot 10^{-12} \cdot R0^{2} \cdot fo^{3} \cdot C \cdot Rdet \qquad [23]$$

Rewriting the equation for Mass Axis voltage from equation [10];

$$Vfb = -\left(\frac{(Daxis)}{65536} \cdot 10\right) - \left(\frac{1}{16} \cdot \frac{(Daxis)}{65536} \cdot 10 \cdot \left(\frac{1}{2} - \frac{Dmgain}{4096}\right)\right) - \left(\frac{1}{200} \cdot 5 \cdot \left(\frac{1}{2} - \frac{Dmoffset}{4096}\right)\right) \qquad [24]$$

Taking the derivative of equation [24] with respect to *Dmgain*,

$$\Delta Vfb = \frac{1}{16} \cdot \frac{(Daxis)}{65536} \cdot \frac{10}{4096} \cdot \Delta Dmgain$$

and the derivative of equation [23] with respect to *fo*,

$$\Delta Vdet = -4 \cdot 7.22 \cdot N \cdot 10^{-12} \cdot R0^2 \cdot C \cdot Rdet \cdot 3 \cdot fo^2 \cdot \Delta fo$$

The Mass gain equation must compensate the detect voltage change. Setting the two equations equal to each other and evaluating at 3276.75 AMU (worst case), the change in frequency compensated for by the full range of *Dmgain* is:

$$\Delta fo|_{max} = -\frac{\left(\frac{1}{16} \cdot \frac{65535}{65536} \cdot \frac{10}{4096} \cdot 4095\right)}{4 \cdot 7.22 \cdot 3276.75 \cdot 10^{-12} \cdot 0.4445^2 \cdot 1.1\times10^{-12} \cdot 486 \cdot 3 \cdot (1\times10^6)^2}$$

The magnitude of the change is;

$$\boxed{\Delta fo|_{max} = 20.8 \text{ Khz}}$$

Therefore, from a nominal frequency of 1.0 Mhz, the mass gain adjustment of +/- 100 AMU compensates for +/- 10 Khz. Furthermore, the AMU gain summation amplifier is weighted the same as the mass gain amplifier, so the AMU gain range also compensates for +/- 10 Khz. Since the entire design is based on 1.0 Mhz, it is best to set the frequency limits to +/- 10 Khz around 1 Mhz.

The relationship or resolution of the mass gain adjustment with respect to a single unit of frequency change is:

$$\Delta Dmgain = -0.1965 \cdot \Delta fo$$

In term of AMU:

$$\Delta MassGain = -9.8263\times10^{-3} \cdot \Delta fo \qquad [25]$$

The units of *fo* are Hz, and the units of *MassGain* are AMU. The same relationship holds for AMU gain. Taking the derivative of equation [15] and applying the same summation term of AMU gain as with mass gain, the following relationship comes out;

$$\Delta AMUGain = 4.8695\times10^{-3} \cdot \Delta fo \qquad [26]$$

The AMU Gain term means that the peaks need widening for an increase in frequency. Widening the peaks implies lowering the U+/U- voltage.

3.9 Page 9 of 18, Octopole

The components on this page generate the control voltages for the octopole assembly G1946-60009. U160 is a dual 12 bit DAC. Channel A controls the RF peak voltage and channel B controls the Knee setting. U153 provides the voltage outputs that are sent to connector P2. The RFPEAK voltage is 0 to -5 volts that corresponds to 0 to 512 volts peak-to-peak on the octopole rods. The O_KNEE voltage is 0 to -5 volts that corresponds to 0 to 4095 AMU. Connector P2 also supplies the power to the octopole assembly. The voltage range out of the DACs are larger than the octopole assembly can handle. The RF peak voltage should be limited to no greater than 300 volts, and the Knee setting should be limited to no greater than 3276.75 since that is the limit of the Mass Axis DAC.

The following table outlines the relationships of the DAC values to the voltages.

Table 6: Octopole Settings

Parameter	Address	Range	Resolution	Relationship
Opole RF Peak	66	0 to 300 v P-P	0.125 mvolt	DAC = 8 * volts
Opole Knee	67	0 to 3276 AMU	1 AMU	DAC = AMU

3.10 Page 10 of 18, FPGA Connection

The center of the page is a Xilinx FPGA, U128. Since the part is SRAM based, the configuration of the part is loaded at power up by a serial PROM U129. U128 is configured for MODE 0 operation which is the basic configuration for serial data. The PROM is programmed with the code from design G1946-80053. All of the input and output connections are shown on the right half of the schematic. The FPGA does all of the decoding, status control, front panel control, and other miscellaneous functions. The following table outlines the registers within the part.

Table 7: FPGA Interface

Parameter	Address	Range	Resolution	Relationship
Status1	0	x	x	16 bit readback
Status2	1	x	x	16 bit readback
Identification	2	x	x	16 bit Identification value
Shutdown Mask	6	x	x	16 bit Mask for Status1

For a complete description of the FPGA design, review the Theory of Operation for G1946-80053.

3.11 Page 11 of 18, DACs

This page contains the DACs and reference voltages for the low voltage lenses on the Analyzer board. The four DACs, U94 through U97, are dual 12 bit multiplying DACs. The opamps, U76 through U79, convert the current out of the DACs to voltages. The relationship of voltage out to Digital word is;

$$Vout = -\left(\frac{Dword}{4096} \cdot Vref\right)$$

For all of the DACs, *Vref* is +10 volts. Therefore, the voltage range out of each DAC is 0 to -10 volts.

The components on the right side of the schematic make up the reference voltages for the low voltage lenses. U90 and U91 are +10 volts references with bypasses on the input and output. Two references were chosen to divide the current drive needed from the references. Also, the layout of the board makes it convenient to use one reference for the IRIS and FRAGMENTOR lenses and the other reference for the remaining lenses. The voltage out of U90 is buffered by U174. The transistors Q110 and Q111 form a switch that kills the reference during a shutdown conditions. This reference drives the IRIS and FRAGMENTOR lenses. By killing the reference, the lenses are driven to ~0 volts. The other lenses are killed by shutting down the power supply for those lenses. Though this is a safe method of turning off the voltages, it is not preferred since the opamps in the lens circuits will rail causing high current draw when the power supply is turned back on. A redesign might consider killing the reference voltage for those lenses.

Opamp U151 is a summation opamp that controls the quad offset voltage. The resistors R614, R623, R624, and R625 are precision resistors that make up a bipolar output. The voltage relationship is:

$$Vdc = -\left(\frac{Rf}{Rin} \cdot Vref\right) \cdot \left(\frac{1}{2} - \frac{Dword}{4096}\right) = -\left(\frac{8k}{10k} \cdot 10\right) \cdot \left(\frac{1}{2} - \frac{Dword}{4096}\right) = -8 \cdot \left(\frac{1}{2} - \frac{Dword}{4096}\right)$$

This is the voltage applied to net QDOFF_DRV which feeds the gain opamps on sheet 3. Using equation [16] and [17] in section 3.3.1, and the above equation,

$$Ua(dc), Ub(dc) = -10 \cdot \left(-8 \cdot \left(\frac{1}{2} - \frac{(Dword)}{4096}\right)\right) = 80 \cdot \left(\frac{1}{2} - \frac{(Dword)}{4096}\right)$$

The following table outlines the DAC to voltage relationship

Table 8: Quad DC

Parameter	Address	Range	Resolution	Relationship
Quad DC	30	-39.98 to +40 volts	0.02 volts	DAC = 2048 - 50 * volts

3.12 Page 12 of 18, Faults

This sheet contains all of the status 2 fault generation. The goal of the fault logic is to sense the condition when the error amps that drive the various lens stages rail. Since all of the error amp designs have a normal operation within +/- 10 volts, any error amp that exceeds +/- 10 volts for an extended amount of time is considered a fault. Using the Skimmer 1 fault logic as an example, the error amp voltage (LV_SK1_TRIP) feeds an RC circuit that delays the input voltage. This delay is used to avoid inadvertent faults due to large voltage steps. During a large voltage step, the error amp may rail for a short amount of time until the control loop is under control. The RC network keeps the fault logic from tripping a fault during this time. The comparator, U81, is configured as a window comparator with a range of -10 to +10 volts. The output of the comparator is an open collector driver. When a fault occurs, the output of the comparator is pulled low. U162 buffers the fault bits. U185 is enabled during a STATUS 2 read. It is also latched during a shutdown condition to avoid any further updates of the status register. The status register is cleared by writing to STATUS 2. U179 in the upper right of the page is the -10 volt reference. All of the comparator circuits are the same except for the quad DC drive fault. The DC drive comes from two opamps on sheet 3. The outputs of both opamps are linked together by the steering diodes CR70 and CR71.

3.13 Page 13 of 18, CAP/IRIS

The components on this sheet drive two voltages, the IRIS and FRAGMENTOR. The FRAGMENTOR is sometimes referred to as the CAP exit voltage. The requirements are for a voltage range of -400 to +400 volts. The rails for these drivers are +/- 450. Using the IRIS driver as an example, the voltage from the IRIS DAC on sheet 11 is feed on the net LV_IRIS. Opamp, U154, is configured as an error amplifier that senses the input and drives the appropriate voltage to get the proper voltage out of the driver. The model of the circuit is as follows:

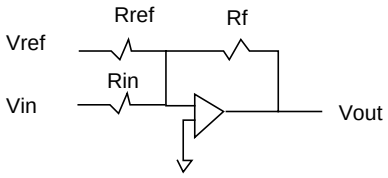

Figure 8: Lens Driver Model

The transfer function is:

$$Vout = -\left(\frac{(Rf)}{Rin} \cdot Vin\right) - \left(\frac{(Rf)}{Rref} \cdot Vref\right)$$

For Rref=2Rin, and substituting the DAC equation;

$$Vout = \frac{Rf}{Rin} \cdot Vref \cdot \left(\frac{Dword}{4096} - \frac{1}{2}\right)$$

For Vref=10 volts;

$$Vout = \frac{Rf}{Rin} \cdot 10 \cdot \left(\frac{Dword}{4096} - \frac{1}{2}\right)$$

This is the basic equation for all of the lens driver circuits. The lens drivers are grouped into two categories, high resolution and low resolution. The high resolution designs have a DAC step of 0.025 volts and the low resolution designs have a DAC step of 0.25 volts.

Therefore, for low resolution designs,

$$\Delta Vout = \frac{Rf}{Rin} \cdot 10 \cdot \frac{1}{4096} = 0.25$$

$$\frac{Rf}{Rin} = 0.25 \cdot \frac{4096}{10} = 102.4$$

The goal of the design is to pick a feedback resistor and a input resistor such that the ratio is 10.24. The feedback resistor was chosen to be 2 Mohm. This minimizes the load of the power supply and worked well with the high impedance of the opamp. Therefore, the input resistor is;

$$Rin = \frac{(Rf)}{102.4} = \frac{(2M)}{102.4} = 19.53 \text{ Kohm}$$

A value of 19.6 Kohm was chosen. For the high resolution designs, the resistor is 196 Kohm.

Following the opamp of the IRIS driver, is a compensation network and a stack of high voltage transistors. The compensation network adds a ZERO at 126 Hz and a POLE at 78 Khz. This compensates for the POLE of the high voltage stage of approximately 125 Hz. Since this design doesn't use optocouplers like the U+/U- design, the first high voltage stage is biased off the high voltage power supply. This first stage has very little current and high impedance that accounts for such a low frequency POLE. Much like the U+/U- amplifier design, the stack of high voltage transistors divide the rail to rail voltage across the collector-emitter pins. The output of the drivers are filtered by some RC networks. The first network is bypassed to ACOM and the second network is bypassed to DCOM. The second network carries most of the capacitance load. The capacitors to DCOM mainly serve to minimize RF coming back on the lens from the manifold elements like the quad (1 Mhz) and octopole (2.5 Mhz). These RF voltages can affect the drivers and cause non-linear voltage gains. The opamp of the driver stage has a compensation network around it that acts like an integrator for low frequencies. The IRIS and FRAGMENOR drivers are identical. The following table outlines the DAC to voltage relationships

Table 9: Iris and Fragmentor

Parameter	Address	Range	Resolution	Relationship
Fragmentor	131	-400v to +400v	0.25 volt	DAC = 2048 + 4 * volts
Iris	28	-400v to +400v	0.25 volt	DAC = 2048 + 4 * volts

3.14 Page 14 of 18, Skimmers

This schematic sheet contains the voltage drivers for Skimmer 1 and Skimmer 2. The analysis of the driver is the same as the IRIS analysis. The difference in this driver is that the rails are lower voltage (~ +/-300 volts) and therefore have fewer high voltage transistors. Furthermore, all of the compensation is around the error amp with a feed forward capacitor to the high and low side of the output voltage stack. The following table outlines the voltage and DAC relationships

Table 10: Skimmer 1 and Skimmer 2

Parameter	Address	Range	Resolution	Relationship
Skimmer1	134	-250v to +250v	0.25 volts	DAC = 2048 + 4 * volts
Skimmer2	135	-51.2v to +51.175v	0.025 volts	DAC = 2048 + 40 * volts

3.15 Page 15 of 18, Lenses

This schematic sheet contains the voltage drivers for Lens1 and Lens2. These are the exact same topology as the skimmer drivers. The following table outlines the voltage and DAC relationships.

Table 11: Lens 1 and Lens 2

Parameter	Address	Range	Resolution	Relationship
Lens1	132	-51.2v to +51.175v	0.025 volts	DAC = 2048 + 40 * volts
Lens2	133	-250v to +250v	0.25 volt	DAC = 2048 + 4 * volts

3.16 Page 16 of 18, Octopole/Supply

This schematic page has one more low voltage driver for the Ion Energy setting that is applied to the octopole assembly. This is the same topology as the other drivers. In the upper right hand corner of the sheet is the DC/DC converter for the drivers. It puts out +/- 300 volts. The input power comes from +24 volts which is filtered by C31, L5, C29, and C30. The output voltages are also filtered by LC components to minimize any switching ripple. Pin 5 of U80 is a fault line that is asserted when the supply has problems maintaining the output voltage. Pin 4 is an enable control line for the supply. If the line is high, then the supply is on. If it is low, then the supply is off. The supply is turned off during a shutdown condition in order to force the lenses to ~zero volts. The following table outlines the voltage and DAC relationship of the ION ENERGY driver.

Table 12: Octopole Ion Energy

Parameter	Address	Range	Resolution	Relationship
Ion Energy	136	-50v to +50v	0.1 volts	DAC = 2048 + 40 * volts

3.17 Page 17 of 18, CAP/APCI

This page contain the interface and control for the capillary voltage, chamber voltage, and APCI current. For the SPRITE design, only one power supply is used to drive the capillary and chamber voltages. Therefore, only one control input is used for the supply. The dual DAC U92 controls the magnitude of the capillary/chamber voltages and the APCI current. U173 are opamps that

convert the current DACs to voltage outputs. P1 is the connector to the capillary/chamber supply. The enable for the supply is controlled by net VCAP_SHUTDN. A low signal turns the supply on and lights up the led DS6. There are two current monitors and one voltage monitor for the capillary/chamber supply. U85 buffers the monitor signals. All monitor signals are protected by 1 Kohm series resistors and 11 volt zener diodes. The 287 Kohm pulldown resistors keep the opamps at zero volts whenever a supply is not connected. The outputs of the buffer opamps are divided to drive a 0 to +5V signal to the ADC. The LEDs, DS1 and DS2, indicate the polarity of the voltage which is controlled by net VCAP_PLRTY. The input control voltage controls the voltage on the capillary while the chamber voltage is offset 500 volts less in magnitude by the power supply. One note about the chamber current readback from P1 pin 16. The voltage level has a different meaning depending on the mode of operation. The power supply senses the polarity and APCI control to determine the scaling of the readback. This is explained further in section 3.18.

The APCI power supply is controlled through connector P3. It has a similar configuration as the capillary/chamber supply in that it has an enable line, a polarity line, a voltage control line, and two readbacks. The readbacks are buffered by U86 and protected by the same series resistance and zener diode. Leds, DS3 and DS4, indicate the polarity of the control current and led DS7 lights when the supply is turned on. The control voltage that determines the amount of current that the APCI needle puts out has two different meanings. The voltage drive to the supply is the same 0 to +10 volts, but the supply interprets the voltage differently depending on the polarity as outlined in the table below.

Both supplies have separate high voltage return connections. Internal to the supply, they are resistively connected to the DCOM lines, however, footprints for stuffing other resistances where placed on the board for experiments through resistors R598, R599, and R600. These components are not loaded at this time.

The following table outlines the voltage and DAC relationships.

Table 13: Capillary voltage and APCI current

Parameter	Address	Range	Resolution	Relationship
Capillary	128	-6000v to +6000v	50 volts	DAC = volts/2.4420
Corona Current Neg. APCI	130	0 to 100uA	0.1 uA	DAC = 40.96 * current[uA]
All other modes		0 to 10uA	0.1 uA	DAC = 409.6 * current[uA]

3.18 Page 18 of 18, Muxed A/D

This page contains the muxed A/D circuitry and the buffers for the RF power readbacks. U87 is an eight channel muxed A/D. Each voltage channel has a range of 0 to +5 volts with voltage and current protection provided by clamping diodes and series resistors. The A/D is configured by firmware to readback single ended analog inputs. The conversions are 8 bit and are driven on the MSE bus during a MUXED A/D read. The enable time of the part is somewhat slow which requires three wait states of the 10 Mhz DSP on smartcard during a read. U86 buffers the power forward and power reflected readbacks from the coil box. The inputs are protected by 1 kohm series resistors and 11 volt zener diodes. The 100 Kohm pulldown resistors keep the outputs at zero volts when the readback cable is not connected. Resistors R448, R449, R447 and R450 allow for scaling, but no scaling was needed. Therefore, R447 and R448 are not loaded. In the current design of SPRITE, the RF power readback cable is not loaded since it seemed to cause some high voltage arcs that damaged the buffer opamps. The protection was added after the cable was removed from the design, so it may be possible to put the readback cable back in with no damage. Currently, the readback is only useful for diagnostic purposes. U88 is a +5 volt linear regulator that supplies power for the A/D and the protection diodes. It also supplies power to the octopole DACs on page 9 of the schematics. The following table outlines all of the eight readbacks of the device. The channel number in the Address column of the table is the data value written to the DAC to configure the channel for single ended operation and to also start a conversion.

Table 14: Muxed A/D Readbacks

Parameter	Address	Range	Resolution	Relationship
APCI Current Readback	34, channel 8			
Neg. APCI		0 to 100 uA	0.392 uA	Value[uA] = 0.392 * A/D
Pos. APCI		0 to 10 uA	0.0392 uA	Value[uA] = 0.0392 * A/D
Vcap Voltage Readback	34, channel 9	0 to 10 KV	0.0392 KV	Value[KV] = 0.0392 * A/D
RF Drive Level Readback	34, channel 10	0 to 100%	0.3922%	Value[%] = 0.3922 * A/D
CAP Current Readback	34, channel 11	0 to 2 uA	7.8 nA	Value[nA] = 7.84 * A/D
Chamber Current Readback	34, channel 12			
Neg. APCI		0 to 100 uA	0.392 uA	Value[uA] = 0.392 * A/D
All other modes		0 to 10 uA	0.0392 uA	Value[uA] = 0.0392 * A/D
APCI Voltage Readback	34, channel 13	0 to 6 KV	39.2 volts	Value[KV] = 0.0392 * A/D
RF Forward Pwr Readback	34, channel 14	0 to 100 Watts	0.392 Watts	Value[W] = 0.392 * A/D
RF Reflected Pwr Readback	34, channel 15	0 to 100 Watts	0.392 Watts	Value[W] = 0.392 * A/D

4.0 Layout Considerations

There are many considerations for the layout of the Analyzer board. The board has many functions and it is quite large in size. Some of the goals of layout are to place functions together as much as possible and to keep power and ground places from cross-talking into other area.

There are two plane layers on the board. One plane layer is dedicated to ACOM and DCOM. The other plane layer carries +5V and +15V. The -15V and +24V power signals are added as fills on signal layers. The ACOM ground is associated with the analog circuitry and the +15V and -15V power signals. The DCOM ground is associated with digital circuitry and the +5V and +24V supplies. The cuts in the planes were made to isolate the digital circuitry from the analog circuitry. Part placement was a big consideration in making the plane cuts fairly straight forward. All of the ground connections are kept separate on the board. The bus board ties all of the grounds together.

The part placement is focused around the circuit functions and the grounding. The lens drivers for the source were placed in the upper left side of the board. All of the components are analog and hence have a large analog plane under them. The power supply was placed next to the drivers. The DACs that drive the lenses are placed along the lower left side of the board. Since digital data lines come into these devices, it was reasonable to keep them near the 96 pin connector. All of the U+/U-, RF control, and other sensitive quad drive circuits were placed in an analog island in the middle of the board. This area has an insulated metal can over it to shield and temperature control the area. The power supplies for the U+/U- circuit were placed to the left of the metal can. This helped block the direct air flow from the fan so that the metal can would not cool from the air. The right side of the board contains the IRIS and FRAGMENTOR lens drivers. They have their own power supplies that are placed to the right of the metal can.

The connectors on the board were located to match with the item connected to them. For example, the CHAMBER/CAP and APCI supply connectors line up with the power supplies in the tub. This was done to keep the cabling as short and direct as possible. The RF output and the IRIS connectors though placed in the proper location, are the only ones that have the possibility of swapping.

The connection types are similar, but different enough to know if the wrong cable is in the connector.

During the design of the board, some of the DACs and the ADC were connected to both ACOM and DCOM. This seemed appropriate because of the amount of digital activity and the philosophy of tying the grounds together at the ADC and DAC. However, the grounds at times would glitch apart and damage the DACs and ADC. Therefore, all of the DACs and ADC are placed on the ACOM plane. The exact cause of the ground separation was never determined, however one possibility is the arcing that occurs in the quad and source.

5.0 Mass Axis and Peak Width Calibration

One of the important goals of the hardware was to make the Mass Axis and Peak Width Calibrations much easier to accomplish than previous designs. With the proper hardware relationships, a user could easily calibrate the peaks through a better understanding and simplification of the calibration parameters of Mass Gain, Mass Offset, AMU gain, and AMU offset. This would also make it very easy for a tune algorithm to accomplish the task of peak calibration in a fraction of the time of past autotune algorithms. In previous instrument designs, the hardware for Mass Gain and Mass Offset came directly from the Mass Axis DAC. That is, the firmware calculated a Mass Axis DAC value from an equation that included Mass Gain and Mass Offset. This process had a number of problems in that there was no direct relationship of gain or offset to the amount of peak adjustment. This made “autotuning” more of a search algorithm that iteratively adjusted the gain and offset terms until the peaks were adjusted. Furthermore, since the Mass Axis DAC was the only means of adjusting the gain and offset terms, the step sizes in the data were erratic, particularly for larger gain values. This occurred because the calculation had to round the calculated value to a mass resolution of 0.05 AMU. As the mass axis was stepped at 0.1 AMU, the mass step size at a certain point would either jump an extra 0.05 AMU or it would repeat the same position. This would leave holes in the data or it would put two data values at the same mass position. In the SPRITE design, hardware DACs were added that performed the Mass Gain and Mass Offset functions. Furthermore, the summation of these functions into the peak position and width summation amplifiers were done in such a way as to provide meaning into the gain and offset terms. As described in section 3.2, the gain and offset terms are in units of AMU which directly relates to the peak position. Once this relationship is established, the calibration is simply a matter of algebra.

5.1 Derivation of Mass Axis calibration

The elements that are controlled in the instrument affect the gain and offset values of a linear calibration curve. The following graph is an example of two linear lines with different slopes and offsets. The slope in this example relates to the gain term.

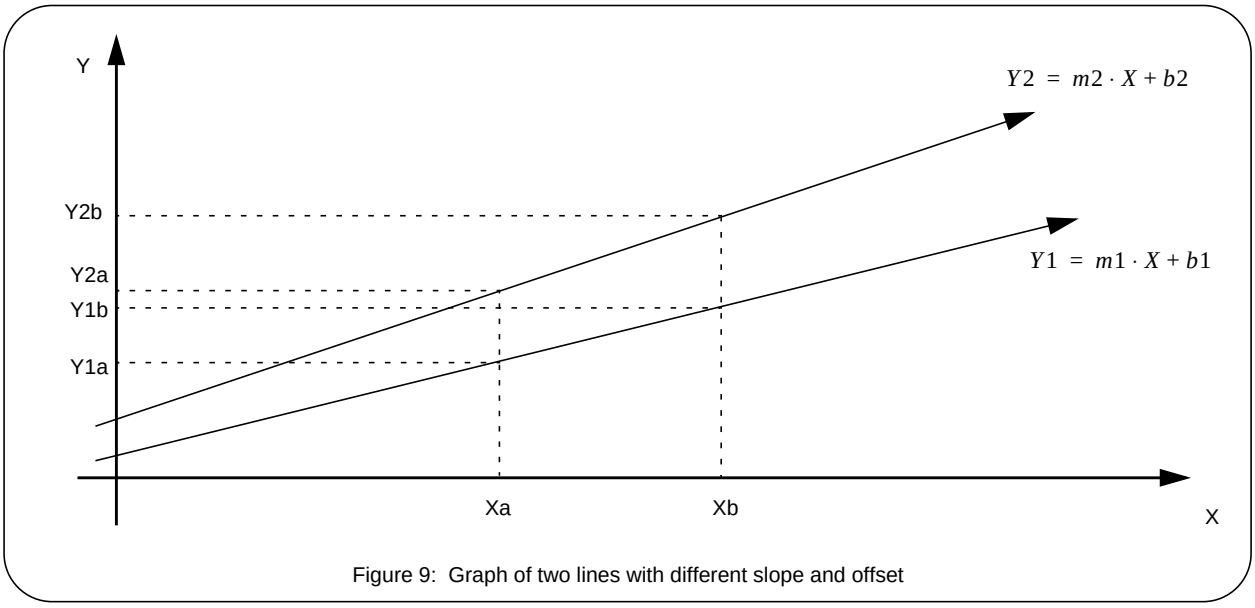

Figure 9: Graph of two lines with different slope and offset

This graph shows two lines of different slope and offset. The goal of the calibration scheme is to make slope and offset corrections to a line, for example Y2, to make it the same as another line, for example Y1. That is, a slope and offset correction must be determined that makes m2 = m1 and b2 = b1.

To start with, take the derivative of the equations of the line.

$$dY2 = m2 \cdot dx$$

$$dY1 = m1 \cdot dx$$

Take the ratio.

$$\frac{dY2}{dY1} = \frac{m2}{m1}$$

$$m2 = \frac{\Delta y2}{\Delta x2}$$

$$m1 = \frac{\Delta y1}{\Delta x1}$$

Substitute.

$$\frac{dY2}{dY1} = \frac{(\Delta y2)/(\Delta x2)}{(\Delta y1)/(\Delta x1)} = \frac{\Delta y2}{\Delta y1} \qquad \text{Where} \qquad \Delta x2 = \Delta x1$$

Therefore, the result.

$$dY2 = \frac{\Delta y2}{\Delta y1} \cdot dY1$$

At this point, a correction factor must be determined that makes the two slopes of the equations the same. The following graph is an example of how the correction factor is determined.

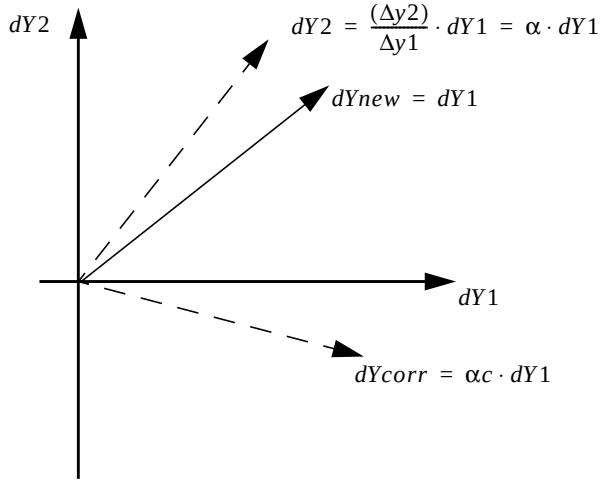

Figure 10: Plot of derivatives and correction factor

Using the graph above, the goal is to find the correction factor, *dYcorr*, such that it will add to the original line, Y2, to create a new line, Ynew, that has the same slope as line Y1. The following equations are derived from the graph.

$$dYnew = dY2 + dYcorr = dY1$$

Therefore,

$$dYnew = \alpha \cdot dY1 + \alpha c \cdot dY1 = (\alpha + \alpha c) \cdot dY1$$

By definition,

$$\alpha + \alpha c = 1 \qquad \{\text{the slopes are equal}\}$$

Therefore,

$$\alpha c = 1 - \alpha = 1 - \frac{(\Delta y2)}{\Delta y1}$$

Substituting,

$$dYcorr = \left(1 - \frac{\Delta y2}{\Delta y1}\right) \cdot dY1$$

Using the values from figure 9,

$$dYcorr = \left(1 - \frac{(y2b - y2a)}{(y1b - y1a)}\right) \cdot dY1$$

This equation determines the amount of correction needed for equation Y2 to make it have the same slope as equation Y1. When this correction is applied, a new line is created as shown on the following graph.

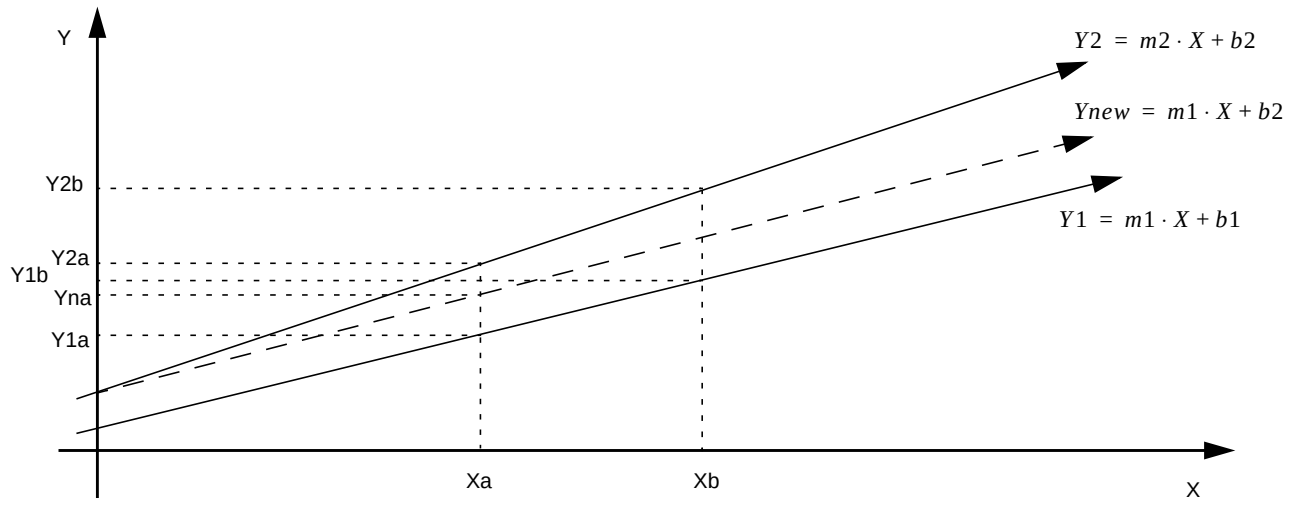

Figure 11: Graph of two lines with different slope and offset

The next step is to determine the offset correction needed to make Ynew the same as Y1. The following equations derive the offset correction factor.

$$yna = dYcorr|_{Xa} + y2a$$

$$bcorr = y1a - yna$$

$$bcorr = y1a - (dYcorr|_{Xa} + y2a)$$

$$bcorr = y1a - \left(1 - \frac{(y2b - y2a)}{(y1b - y1a)} \cdot dY1|_{Xa} + y2a\right)$$

The derivative of Y1 evaluated at Xa is simply the value Y1a. Substituting Y1a for dY1 gives the following.

$$bcorr = y1a \cdot \left(\frac{y2b - y2a}{y1b - y1a}\right) - y2a$$

The equation determines the offset correction needed to make the new line, Ynew, the same as Y1.

In summary, given two lines of different slopes and offsets, one can determine the change in gain and offset needed to make the two lines the same. The proof is a very generalized relationship using generic slopes and offsets. For mass spectrometry, the goal would be to correlate the gain and offset corrections to direct control functions of the instrument.

5.2 Application for Mass Gain and Offset Adjustment

Our typical method of tuning an instrument is to setup some known peak positions in a tune file and make adjustments to the instrument such that the profiled tune masses are aligned with the given positions. The peak positions that are used in the tune file are in units of AMU. Therefore, if the derived relationships of adjusting gain and offset were in units of AMU, the instrument could be tuned by simply determining the current positions of the mass peaks versus the desired tune positions and calculate the adjustment needed for mass gain and mass offset. From section 3.2, the hardware was designed to make the mass gain and mass offset in units of AMU. This makes it very easy to tune the peak positions.

Using the two correction equations for gain and offset,

$$dYcorr = \left(1 - \frac{(y2b - y2a)}{(y1b - y1a)}\right) \cdot dY1$$

$$bcorr = y1a \cdot \left(\frac{y2b - y2a}{y1b - y1a}\right) - y2a$$

The elements are as follows.

Table 15: Mass Gain and Offset Elements

Element	Description
y1a	Low mass desired position in AMU (tune file)
y1b	High mass desired position in AMU (tune file)
y2a	Low mass actual position in AMU (from profile)
y2b	High mass actual position in AMU (from profile)
dY1	3276.8 AMU (adjustment location from hardware)
dYcorr	Gain adjustment at 3276.8 AMU (from hardware)
bcorr	Offset adjustment in AMU (for all masses)

5.2.1 Mass correction example 1:

In this example, the tune masses of interest are 69.0 AMU and 502.0 AMU. Therefore, these peak positions are in the tune file and are considered the desired positions. Lets assume that the instrument was turned on and profiled giving the peak positions of 69.15 AMU and 506.35 AMU. Lets also assume that there is no current mass gain and mass offset applied. What would be the new gain and offset corrections needed to tune the instrument to the desired peak positions?

$$dYcorr = \left(1 - \frac{(506.35 - 69.15)}{(502.0 - 69.0)}\right) \cdot 3276.8 = -31.78 \text{ AMU}$$

$$bcorr = 69 \cdot \left(\frac{506.35 - 69.15}{502.0 - 69.0}\right) - 69.5 = 0.17 \text{ AMU}$$

These calculated values are the values applied to the mass gain and offset adjustments since there are no current adjustments applied. One interesting aspect of this example is that tune masses from the profile windows were both high. One might assume that the mass offset needs a negative adjustment. The calculations show that the offset correction is positive. This happened because the gain needed so much adjustment to correct the mass positions.

5.2.2 Mass correction example 2:

Lets assume that the same conditions apply as in example 1, except that there is already a mass gain value of +27.33 AMU and an offset value of +1.29 AMU in the tune file. What are the new gain and offset values?

$$dYcorr = \left(1 - \frac{(506.35 - 69.15)}{(502.0 - 69.0)}\right) \cdot 3276.8 = -31.78 \text{ AMU}$$

$$bcorr = 69 \cdot \left(\frac{506.35 - 69.15}{502.0 - 69.0}\right) - 69.5 = 0.17 \text{ AMU}$$

The same calculations occur to determine the adjustments needed for the peaks. These adjustments are then added to the current adjustments.

$$dYnew = -31.78 + 27.33 = -4.45 \text{ AMU}$$

$$bnew = 0.17 + 1.29 = 1.46 \text{ AMU}$$

These new values are the values that are applied for mass gain and mass offset.

5.3 Derivation of AMU Gain and Offset Calculations

The derivation of AMU gain and offset is different from the Mass gain and offset derivation. The correction factors for Mass gain and offset have a difference term in the denomination. Since the tune peaks are at different locations, the denominator is never zero. However, if the same equations are applied to peak width, the denominator term would be zero since the peak widths might require the same value at different masses. In a typical application, the peak widths would be the same across the entire mass range. Therefore, there is a slight variation to the derivation of AMU gain and offset.

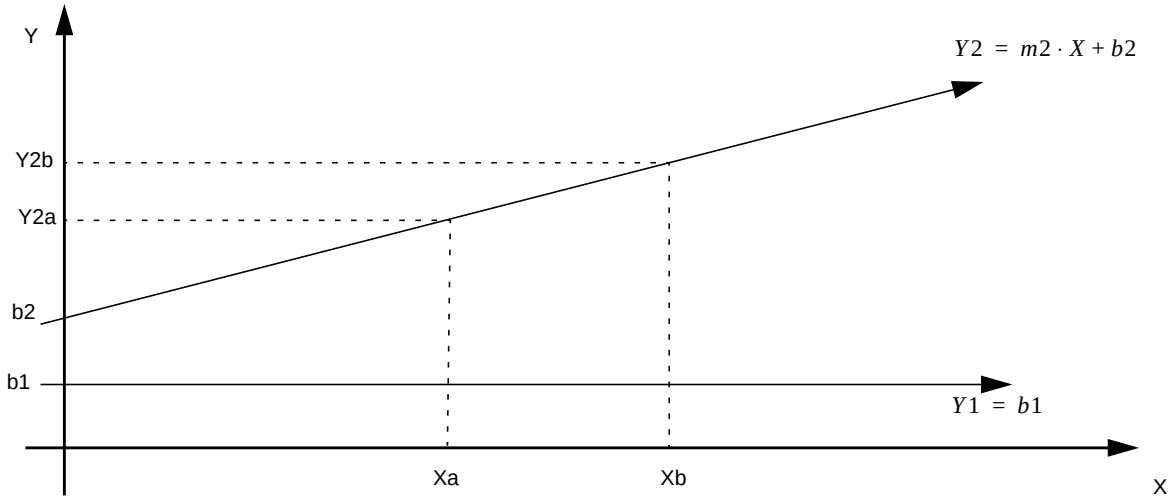

Figure 12: Graph of two lines with different slope and offset

Figure 12 represents a typical approach to solving the AMU gain and offset adjustment calculation. The line Y1 represents the desired result where b1 is the desired peak width. Since the desired result will most likely have the same peak width across the mass range, Y1 has no slope. Y2 represents the actual peak width where m2 and b2 are gain and offset terms.

To start with, take the derivative of the equation for Y2

$$dY2 = m2 \cdot dx$$

the slope is:

$$m2 = \frac{Y2b - Y2a}{Xb - Xa}$$

The goal now is to create a correction factor such that a new line is achieved with no slope.

$$dYnew = dY2 + dYcorr = 0$$

$$dYcorr = -dY2 = -m2 \cdot dx$$

Substituting for slope

$$dYcorr = -\frac{Y2b - Y2a}{Xb - Xa} \cdot dx$$

This equation determines the amount of correction needed for equation Y2 to have the same slope as Y1. When the correction is applied, a new line is created as shown on the following graph.

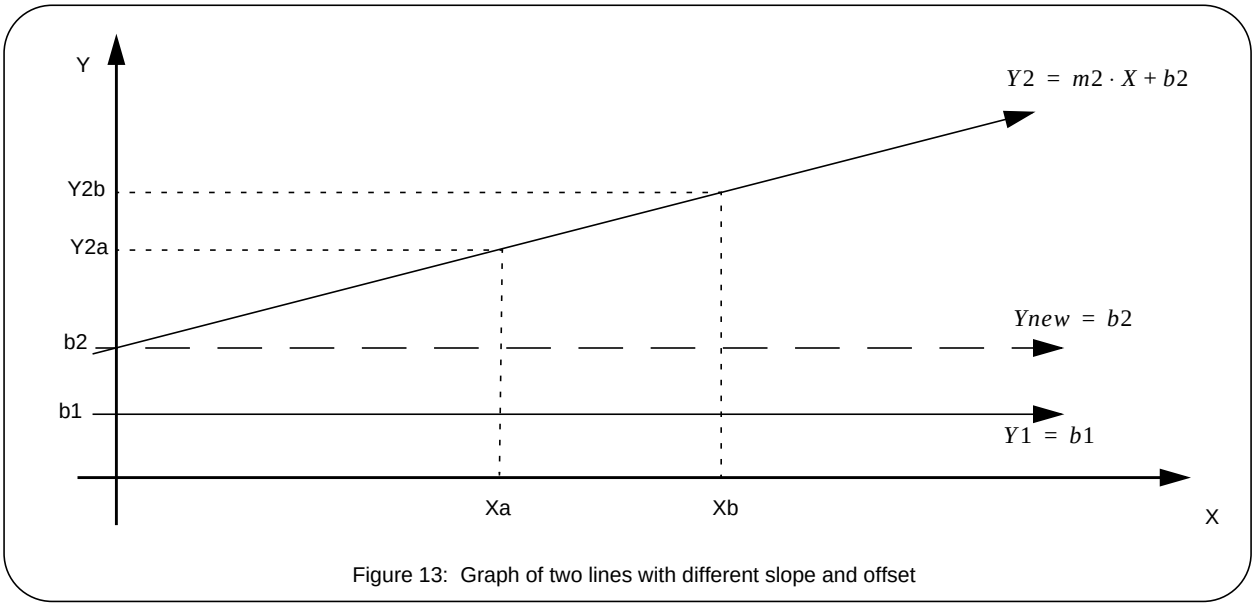

Figure 13: Graph of two lines with different slope and offset

The next step is to determine the offset correction needed to make Ynew the same as Y1. The following equations derive the offset correction factor.

$$b2 = Y2a + dYcorr|_{Xa}$$

$$bcorr = b1 - b2$$

$$bcorr = b1 - (Y2a + dYcorr|_{Xa})$$

$$bcorr = b1 - Y2a + \frac{Y2b - Y2a}{Xb - Xa} \cdot dx|_{Xa}$$

The value of dx evaluated at Xa is simply Xa. Therefore,

$$bcorr = b1 - Y2a + \frac{Y2b - Y2a}{Xb - Xa} \cdot Xa$$

This equation determines the amount of offset correction needed to make the new line, Ynew, the same as Y1.

5.4 Application for AMU Gain and Offset Adjustment

Our typical method of tuning the peak widths is to profile the tune peaks and adjust the AMU gain and offset parameters until the peak widths are the same for all masses. In past instruments, the algorithm was an iterative search trying to converge on the proper gain and offset terms. Using the mathematical model of gain and offset, profile results are used with the desired results in the calculation to determine the amount of peak width adjustment needed. From section 3.2, the hardware was designed to make the adjustments of gain and offset in units of AMU. This makes it very easy to tune the peak widths.

Using the two equations for gain and offset,

$$dYcorr = -\frac{Y2b - Y2a}{Xb - Xa} \cdot dx$$

$$bcorr = b1 - Y2a + \frac{Y2b - Y2a}{Xb - Xa} \cdot Xa$$

the elements are as follows:

Table 16: AMU Gain and Offset Elements

Element	Description
Y2a	Low mass actual peak width in AMU (tune file)
Y2b	High mass actual peak width in AMU (tune file)
Xa	Low mass peak position in AMU (from profile)
Xb	High mass peak position in AMU (from profile)
b1	desired peak width for all masses (tune file)
dx	3276.8 AMU (adjustment location from hardware)
dYcorr	Gain adjustment at 3276.8 AMU (from hardware)
bcorr	Offset adjustment in AMU (for all masses)

There are several draw backs to using the calibration equations for peak widths. If the profile data does not find any peaks, the peak width adjustments may be applied too high causing the peak widths to narrow beyond the capability of the instrument and the peak is simply gone. Therefore, there is no way to apply the calculations since there is no actual peak width values of any meaning. The only way to apply the calculation is to have broader peaks than the desired or to have narrower peaks, but within the resolution performance of the instrument. This will allow for meaningful values to be used in the calculations.

Another problem with the calculations is that the relationship of AMU gain and offset adjustments to the actual peak width change are not exact. Though a model is used for determining the adjustments, a certain amount of error may occur due to the performance of the instrument in general. If the instrument has a very high resolution (i.e. good quad, source, and detector), then the model is more accurate. As the performance of the instrument degrades, the model is less accurate and could lead to improper adjustments. Furthermore, the adjustments assume a linear relationship of peak width. This is true for small changes in adjustment, however, for large changes in peak width, the relationships are not quite linear. The peak width change has a second order affect that starts to dominate the peak width adjustment. Furthermore, the peak width adjustments are not linear across the mass range. The resolution of the adjustments at higher mass are less effective than at lower mass. Because of these effects, the calculations are not as accurate as hoped for.

The last known problem with peak width adjustment calculations has to do with the method of calculating peak width in the profile window. The current method calculates the half-height of the peak and finds this value on both sides of the peak. Once it finds the locations, it calculates the peak width by measuring the distance between the two half-height points. This method works very well assuming there are no other peaks interfering with the “main” tune peak. Essentially, no isotopes. This is shown in the following figure.

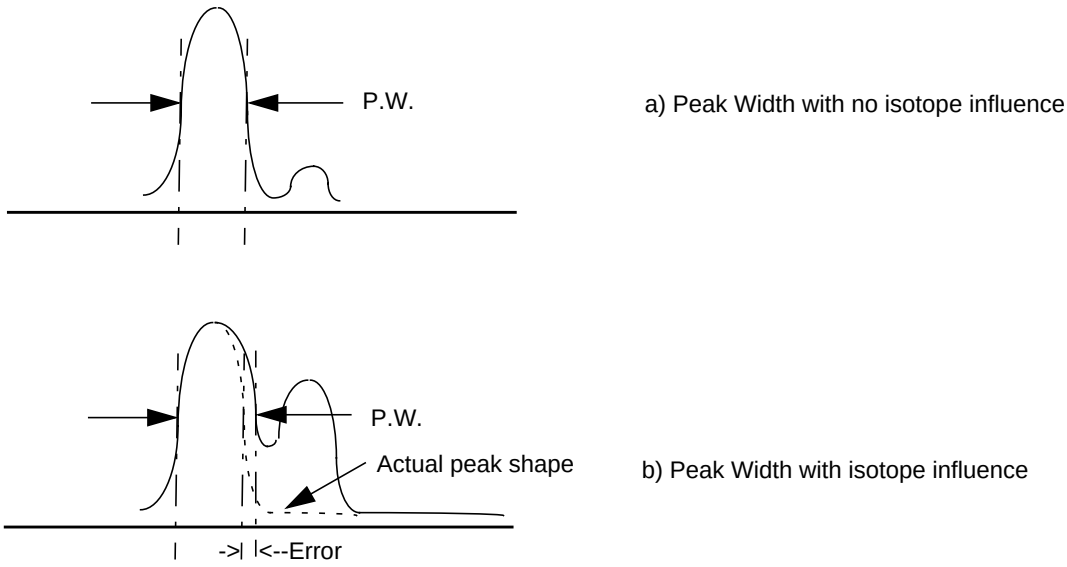

Figure 14: Peak Width calculation wiith and without isotope influence

However, when an isotope of N+1 exists, its begins to interfere with the calculated peak width. As the N+1 peaks get large relative to the main peak, it starts to influence the peak width calculation. This makes the main peak appear broader than it really is. Therefore, the peak width calculation at half-height has an error that is proportional to the abundance of the isotope as shown in figure 14b.

Therefore, caution should be used when using the mathematical relationship. When the second order affects are added to the model, the performance of the instrument exceeds the desired performance of the tune, and a more intelligent peak width calculation is developed, then the mathematical calculations for AMU gain and offset can be used more extensively.

5.4.1 AMU gain and offset example 1:

Lets assume that the desired peak widths for all masses is 0.6 AMU. The tune masses of interest are 69.0 AMU and 502.0 AMU. The instrument is turned on and profiled. From the profile windows, the peak widths for mass 69 and 502 are 0.6 AMU and 1.2 AMU respectively. Let's assume that there are no current peak width gain and offset corrections applied. What are the desired peak width adjustments needed?

$$dYcorr = -\frac{1.2 - 0.6}{502 - 69} \cdot 3276.8 = -4.54 \text{ AMU}$$

$$bcorr = 0.6 - 0.6 + \frac{1.2 - 0.6}{502 - 69} \cdot 69 = 0.096 \text{ AMU}$$

These corrections represent the amount of change needed for the AMU gain and offset adjustments. Mathematically, the sign of the gain term is negative to represent a change that is opposite the "positive" slope of the profiled peaks. From the peak width data, the peak widths are more positive for higher masses, therefore the correction needed is negative. The sign of the offset adjustment is positive to mean that more peak width is needed.

Since the AMU gain and offset adjustments for SPRITE are in units of DAC counts, the calculated values need converting to DAC counts. The direct conversions are listed in the following table

Table 17: AMU Gain & Offset Conversions

Parameter	Conversion
AMU Offset	DAC = 2048 + bcorr/0.002
AMU Gain	DAC = 2048 + dYcorr/0.05

Therefore, the correction factors in DAC counts are:

{ Gain value } $$DAC = 2048 + \frac{(-4.54)}{0.05} = 1957$$

{ Offset value } $$DAC = 2048 + \frac{(0.978)}{0.002} = 2537$$

Now, using Table 4, convert the DAC values (range of 0 to 4095) back to the units used in the host software (range of -2047 to +2047).

{ Gain value } $$\# = -(DAC - 2048) = -(1957 - 2048) = 91$$

{ Offset value } $$\# = -(DAC - 2048) = -(2537 - 2048) = -489$$

5.4.2 AMU gain and offset Example 2:

Suppose that the desired peak width is 0.6 AMU. The tune masses of 69 AMU and 502 AMU have peak widths of 0.95 and 0.75 respectively. Lets also assume that the gain parameter has a current value of -20.5 AMU and the offset has a value of -1.36 AMU. What are the new AMU gain and offset values?

Calculate the gain and offset corrections.

$$dYcorr = -\frac{0.75 - 0.95}{502 - 69} \cdot 3276.8 = 1.51 \text{ AMU}$$

$$bcorr = 0.6 - 0.95 + \frac{0.75 - 0.95}{502 - 69} \cdot 69 = -0.382 \text{ AMU}$$

The DAC counts are calculated and added to the existing settings.

{ new Gain value } $$(-20.5) + (1.51) = -19.00 \text{ AMU}$$

{ Gain DAC value } $$DAC = 2048 + \frac{(-19.00)}{0.05} = 1668$$

{ new Offset value } $(-1.36) + (-0.382) = -1.742$ AMU

{ Offset DAC value } $$DAC = 2048 + \frac{(-1.742)}{0.002} = 1177$$

The host software settings are:

{ Gain value } $\# = -(DAC - 2048) = -(1668 - 2048) = 380$

{ Offset value } $\# = -(DAC - 2048) = -(1117 - 2048) = 931$

5.5 Using Mass Axis and Peak Width Calibration

The concepts and mathematical models developed in the previous section are very useful in tuning an instrument. Previous instrument designs relied on iterative methods to converge to the correction adjustments. With Sprite, the adjustments are simply a matter of determining what you have and calculating the correction you need. Even if the instrument needs redipping by changing the frequency, the calculations for new mass gain and AMU gain value can be done quickly and applied to keep the instrument tuned as shown with equations [25] and [26]

5.5.1 Frequency change example

Lets assume that the instrument had well tuned peaks, but was in need of redipping. If the frequency changed from 1.001 Mhz to 997 Khz, what are the new Mass gain and AMU gain values needed to correct the peak assignments and peak widths?

From equations [25] and [26];

$$\Delta MassGain = -9.8263\times10^{-3} \cdot (-4\times10^{3}) = 39.31 \text{ AMU}$$

$$\Delta AMUGain = 4.8695\times10^{-3} \cdot (-4\times10^{3}) = -19.478 \text{ AMU}$$

The change in DAC setting for peak width is:

$$\Delta DAC = -\frac{19.478}{0.05} = 390$$

The change in host setting is:

$$\Delta\# = -390$$

6.0 Temperature Effects

One of the important performance specifications of the instrument is to be stable over the operating range of +15C to +35C. This is the typical marketing specification that is presented to customers with a certain understanding that the ambient air should be

kept within this temperature range (59F to 95F). This type of performance specification requires that the peak performance (position, width, abundance, ect.) should remain stable through this temperature range, or at least remain within a certain tolerance of stability. The goal of this section is to calculate the performance specification required on electrical components to meet the stability needed within the temperature range

6.1 Temperature effects on Mass Axis

There are essentially three areas that contribute to the stability of the peak position; 1) Mass Axis summation amplifier, 2) RF Detect circuit, and 3) the quad frequency. Each of these areas are reviewed in the following sections to determine their performance requirements.

6.1.1 Summation Amplifier

The summation amplifier components are all of the components that are summed into the mass axis summation amplifier circuit of schematic sheet 2. All of the DACs and the resistors that sum into the mass axis amplifier play a role in determining the stability of the instrument. The goal of meeting the stability criteria is to select DACs, opamps, and resistors that do not cause errors due to temperature effects.

Using figure 1 of section 3.2.4 as the basis for analyzing temperature effects, the summation equation is written keeping the resistor terms and substituting the DAC equations to come up with:

$$Vfb = -\frac{R2}{R1}\cdot Vaxis - \left(\frac{R2}{R3}\cdot Vaxis + \frac{R2}{R4}\cdot\frac{-Dmgain}{4096}\cdot Vaxis\right) - \left(\frac{R2}{R5}\cdot Vref + \frac{R2}{R6}\cdot\frac{-Dmoffset}{4096}\cdot Vref\right) \qquad [27]$$

From this equation, the effects of the voltage reference, the resistors, and the DACs are determined. Each effect of an element is determined by taking the derivative of *Vfb* with respect to the element. Then, the ppm/C requirement is determined by assuming no greater than a 0.05 AMU error over 20C.

Using R1 as an example, the derivative is:

$$\frac{d}{dR1}Vfb = \frac{(R2\cdot Vaxis)}{R1^2} = \frac{(10k\cdot 10v)}{10k^2} = 1mV/\Omega$$

Since the drift must remain within 0.05 AMU, the value above converts to:

$$\Delta\Omega = \frac{(10V)/65536}{(1mV)/\Omega} = 0.153\Omega$$

Using a change of temperature of 20C, this value translates to a ppm/C figure of:

$$ppm/C = \frac{0.153\Omega}{10k\Omega}\cdot\frac{(1\times10^6)}{20C} = 0.765\,ppm/C$$

This process is repeated for all of the elements in equation [27]. The following table is the results.

Table 18: Temperature affects for Mass Axis summation amplifier

Element	Change/Unit	Delta Unit	ppm/C
R1	+1000 uV/Ohm	0.153 Ohm	0.765
R2	-1000 uV/Ohm	0.153 Ohm	0.765

Table 18: Temperature affects for Mass Axis summation amplifier

Element	Change/Unit	Delta Unit	ppm/C
R3	+0.977 uV/Ohm	156.2 Ohm	24.4
R4	0 to -3.9 uV/Ohm	min. 39 Ohm	12.2
R5	+0.0125 uV/Ohm	12.2kOhm	305
R6	0 to -0.050 uV/ Ohm	min, 3.1kOhm	155
Dmgain	152.6 uV/Count	1 Count	12.2
Dmoffset	12.2 uV/Count	12.5 Counts	152.6
Vref	+/- 5000 uV/Volt	31mV	310

The importance of the table is the PPM/C values. If temperature gradients of 20C are expected, then the resistors must meet the PPM/C calculated values to avoid any more than 0.05 AMU shift. However, there are a few things that help this situation. For one, if the temperature gradients were kept within 10C instead of 20C, then the PPM/C values could double. This would make it a bit easier to qualify parts. Furthermore, the sign of the CHANGE/UNIT column is very important. For example, the resistors R1 and R2 have opposite effects. Therefore, if the two resistors had the same PPM/C value and both experienced the same temperature change, then they would cancel each other out. Another effect is the DAC value applied to the Mass Gain and Mass Offset DACs. If the DACs have a value of 2048, which is the nominal value applied for no adjustment in the gain and offset circuits, then the temperature effects of the resistors further cancel each other out. As gain and offset are applied to the instrument for calibration, the temperature effects start to add to the stability relationship. Therefore, the more gain and offset adjustment needed for an instrument, the more the temperature effects have on the stability.

With this knowledge, the resistors R1 and R2 were chosen as a matched pair in the same package to keep the differential effects minimum. The resistors R3/R4 and R5/R6 were chosen such that R3 is actually two R4s and R5 is actually two R6s. By using the same resistors, there is a better chance that the PPM/C effects will cancel each other out. All of the resistors are placed in a temperature controlled zone enclosed by a metal shield. This helps keep gradients minimum and also keeps absolute temperature changes minimum. Lastly, the detect circuit for the RF loop and the gain resistor for the U+/U- amplifier were chosen such that the DAC values nominally start at 2048 to minimize their effects.

6.1.2 RF Detect circuit

Other than the diodes that are compensated with the diode correction circuit, there are two elements that have a direct impact on the RF voltage stability; 1) the sampling capacitor, and 2) the detect resistor. Typically, the RF peak voltage determines the mass position. Therefore, if the RF peak voltage changes, the peak position will change. However, if the U+/U- circuit does not change for a given change in RF peak voltage, then the peak width will also change. Therefore, it is very important that the RF peak voltage be stable with temperature.

Using equation [23];

$$Vdet = -4 \cdot 7.22 \cdot N \cdot 10^{-12} \cdot R0^2 \cdot fo^3 \cdot C \cdot Rdet$$

To evaluate the effects of the sampling capacitors, take the derivative with respect to *C*;

$$\frac{d}{dC} Vdet = -4 \cdot 7.22 \cdot N \cdot 10^{-12} \cdot R0^2 \cdot fo^3 \cdot Rdet$$

For *N*=3276.75 AMU, *R0*=0.4445 in., *Rdet*=476.5 Ohm, and *fo*=1x10^6 Mhz, this equates to,

$$\frac{d}{dC}Vdet = -8.909V/pF$$

If the goal is to be stable within 0.05 AMU, then

$$\Delta C = \frac{(10V)/65536}{(8.909V)/(pF)} = 17.127\times10^{-6}pF$$

Using a change of temperature of 20C, this value translates to a ppm/C figure of:

$$ppm/C = \frac{17.127\times10^{-6}pF}{1.1pF}\cdot\frac{(1\times10^{6})}{20C} = 0.779ppm/C$$

Now, looking at the effects of the resistor, *Rdet*, take the derivative with respect to *Rdet*.

$$\frac{d}{dRdet}Vdet = -4\cdot7.22\cdot N\cdot10^{-12}\cdot R0^{2}\cdot fo^{3}\cdot C$$

This evaluates to;

$$\frac{d}{dRdet}Vdet = -20.567mV/\Omega$$

If the drift must remain within 0.05 AMU, the value above converts to:

$$\Delta\Omega = \frac{(10V)/65536}{(20.567mV)/\Omega} = 0.0074\Omega$$

Using a change of temperature of 20C, this value translates to a ppm/C figure of:

$$ppm/C = \frac{0.0074\Omega}{476.5\Omega}\cdot\frac{(1\times10^{6})}{20C} = 0.776ppm/C$$

Essentially, the sampling capacitors and the detection resistor need tight absolute tolerances since the detect circuit does not have any type of cancellation scheme that occurs in the summation amplifier. The sampling capacitor used in Sprite is an in-house design that has a very well known temperature coefficient. The resistor, R475 of sheet 4, is summed with a negative Tc resistor, RT5 on assembly G1946-60005, to compensate for temperature drift of the sampling capacitor. Furthermore, the sampling capacitor is heated and temperature controlled to minimize the temperature drift of the part. As for the detect resistor, it must have a low ppm/C value. The only compensation on the analyzer board is from placing the resistor within the heated zone.

6.1.3 Quad Frequency on Mass Assignment

The frequency of the Quad RF signal plays an important role in the peak stability of the instrument. A change in frequency due to temperature drift can cause two different effects; 1) peak assignment shift, and 2) peak width shift. This section will deal with the peak assignment shift.

Using equation [23],

$$\frac{d}{df}Vdet = -4\cdot7.22\cdot N\cdot10^{-12}\cdot R0^{2}\cdot C\cdot Rdet\cdot3\cdot fo^{2} = (29.401uV)/(Hz)$$

Since the drift must remain within 0.05 AMU, the value above converts to:

$$\Delta Hz = \frac{(10V)/65536}{(29.401uV)/(Hz)} = 5.190Hz$$

Using a change of temperature of 20C, this value translates to a ppm/C figure of:

$$ppm/C = \frac{5.190Hz}{1Mhz} \cdot \frac{(1\times10^6)}{20C} = 0.260ppm/C$$

Since the DDS circuit is a digital divider of a base frequency, this requirement is placed on the crystal oscillator which is 20 Mhz. Most crystals are specified over the 0 to 60C temperature range. Therefore, the crystal needs to have an accuracy of 5.190 Hz over 20C or 15.570 Hz over 60C (15.57 ppm). The crystal used on SPRITE is a 100 ppm over 70C which is equivalent to ~85.7 ppm over 60C. The current design is off by a factor of five. At the time of the SPRITE release to manufacturing, the specification on the crystal oscillator was not known and therefore, these requirements are not met with the current design.

The following table is a summation of all of the elements on peak assignment stability.

Table 19: Temperature affects for Mass Axis stability

Element	Change/Unit	Delta Unit	ppm/C
R1	+1000 uV/Ohm	0.153 Ohm	0.765
R2	-1000 uV/Ohm	0.153 Ohm	0.765
R3	+0.977 uV/Ohm	156.2 Ohm	24.4
R4	0 to -3.9 uV/Ohm	min. 39 Ohm	12.2
R5	+0.0125 uV/Ohm	12.2kOhm	305
R6	0 to -0.050 uV/ Ohm	min, 3.1kOhm	155
Dmgain	152.6 uV/Count	1 Count	12.2
Dmoffset	12.2 uV/Count	12.5 Counts	152.6
Vref	+/- 5000 uV/Volt	31mV	310
Sampling Cap	-8.909 V/pF	17.127x10-6 pF	0.779
Detect Resistor	20.567 mV/Ohm	0.0074 Ohm	0.776
Crystal	29.401 uV/Hz	5.190 Hz	0.260

6.2 Peak Width Stability

Similar to peak assignment, there are elements that affect peak width. The main elements that affect peak width are 1) AMU summation amplifier, 2) U+/U- amplifier, and 3) the quad frequency.

6.2.1 Temperature effects on AMU summation amplifier

The same analysis applied to the mass axis summation amplifier, applies to the AMU summation amplifier. The results are the same with the same PPM/C values. Therefore, the same resistors, references, and DACs were used for the AMU summation amplifier. All of these parts were also placed within the temperature controlled zone.

6.2.2 Temperature effects of the U+/U- amplifier.

The area of most concern with the U+/U- amplifier is the low voltage stage. This contains all of the precise resistors and opamps to control the output voltage. Start with the equation for the output voltages from equations [11] and [12].

$$Ua = -Vin \cdot \left(\frac{R1}{R7} + \frac{R1}{R3} + \frac{R1}{R6}\right) - \left(Vdc \cdot \frac{R1}{R4}\right)$$

$$Ub = Vin \cdot \left(1 + \frac{R2}{R3} + \frac{R2}{R5}\right) - \left(Vdc \cdot \frac{R2}{R5}\right)$$

To determine the change in output voltage with respect to one of the resistors, take the derivative. For example, the derivative of *Ua* with respect to *R3*, and *Ub* with respect to *R3* is:

$$\frac{d}{dR3}Ua = \frac{(Vin \cdot R1)}{R3^2} = \frac{(-10V \cdot 2M\Omega)}{29.4k\Omega^2} = -23.14mV/\Omega$$

$$\frac{d}{dR3}Ub = -\frac{(Vin \cdot R2)}{R3^2} = -\frac{(-10V \cdot 2M\Omega)}{29.4k\Omega^2} = 23.14mV/\Omega$$

Since the drift must remain within 0.05 AMU, the value above converts to:

$$\Delta\Omega = \frac{(783.3915V)/65536}{(23.14mV)/\Omega} = 0.517\Omega$$

Using a change of temperature of 20C, this value translates to a ppm/C figure of:

$$ppm/C = \frac{0.517\Omega}{29.4k\Omega} \cdot \frac{(1\times10^6)}{20C} = 0.879ppm/C$$

This process is repeated for all of the elements in equations [11] and [12]. The following table is the results.

Table 20: Temperature affects for U+/U- amplifier

Element	From Vin uV/Unit	From Vdc uV/Unit	From Vin Delta Unit	From Vdc Delta Unit	From Vin ppm/C	From Vdc ppm/C
R1 (Ua)	+395.14 /Ohm	-/+ 20	30.25 Ohm	598 Ohm	0.756	15
R2 (Ub)	-390.14 /Ohm	-/+ 20	30.64 Ohm	598 Ohm	0.766	15
R3 (Ua,Ub)	-/+ 23140 /Ohm		0.517Ohm		0.879	

Table 20: Temperature affects for U+/U- amplifier

Element	From Vin uV/Unit	From Vdc uV/Unit	From Vin Delta Unit	From Vdc Delta Unit	From Vin ppm/C	From Vdc ppm/C
R4 (Ua)		+/- 200 /Ohm	Ohm	59.8		15
R5 (Ub)	+500 /Ohm	+/-200 /Ohm	23.9 Ohm	59.8	5.98	15
R6 (Ua)	-5 /Ohm		2.39kOhm		59.8	
R7 (Ua)	-500 /Ohm		23.9 Ohm		5.98	

The specifications from this table are tough. Almost every resistor needs a tight tolerance in temperature. As with the summation amplifiers in sections 6.1.1 and 6.2.1 there are a few things that can lighten up on the specification. First of all, if the temperature gradients in the circuit are lower than 20C, then the PPM/C ratings can increase. Also, the amplifier topology has some features that can make the resistor changes cancel out. For example, If R1,R2, and R3 can track each other in temperature and if they had the same temperature coefficient, then R3 will mainly cancel the effects of R1 and R2. Furthermore, if R5, R6, and R7 are coupled, then they will also cancel each other out in temperature drift. Finally, the specification for peak width of 0.05 AMU is probably a bit tight. Sprite has a relaxed specification at high mass and typically, the change in voltage to get 0.05 AMU change at high mass is a bit larger in practice than the theoretical value.

Therefore, the amplifier resistors are placed inside of a temperature controlled zone. The current resistors are discrete and in separate packages, so the specifications are very tight (2 ppm/C). In future revisions, it might be advisable to use a signal part with multiple resistors to make up R1, R2 and R3. If they are of the same technology and in the same package, the effects of temperature will cancel out.

One thing to note in the table above. The table was split in to two area; 1) the effects due to *Vin*, and 2) the effects due to *Vdc*. The *Vin* term is the important term in determining peak width change. The *Vdc* term cause the same voltage change on both outputs which does not have the same effect on peak width, therefore, it is not as important.

6.2.3 Temperature effects on frequency.

As stated in section 6.1.3, the frequency has an effect on peak assignment. However, it also affects peak width. When the frequency changes, a new U+/U- voltage is needed on the quad. The analysis for the DC voltage on the quad comes from the Mathieu equation. By analyzing the Mathieu equation, the amount of frequency variation allowed for a 0.05 AMU peak width change can be determined.

Start with equation [15]

$$Udc = 1.21 \cdot N \cdot 10^{-12} \cdot fo^2 \cdot R0^2$$

Taking the derivative with respect to frequency,

$$\frac{d}{df} Udc = 1.21 \cdot N \cdot 10^{-12} \cdot 2 \cdot fo \cdot R0^2 = (1.5668mV)/(Hz)$$

Since the drift must remain within 0.05 AMU, the value above converts to:

$$\Delta Hz = \frac{(783.3915V)/65536}{(1.5668mV)/(Hz)} = 7.629Hz$$

Using a change of temperature of 20C, this value translates to a ppm/C figure of:

$$ppm/C = \frac{7.629Hz}{1Mhz} \cdot \frac{(1\times10^{6})}{20C} = 0.381ppm/C$$

As mentioned in section 6.1.3, the constraint on the frequency drift due to temperature was not known. This specification is difficult to meet with standard crystal oscillators.

6.3 Temperature drift from a change in R0

One last aspect to consider is the temperature coefficient for the *R0* value. This is calculated by taking the derivative of the detect voltage for the RF loop and the Mathieu DC equation for the U+/U- voltages.

$$\frac{d}{dR0}Vdet = -4 \cdot 7.22 \cdot N \cdot 10^{-12} \cdot 2 \cdot R0 \cdot C \cdot Rdet \cdot fo^{3} = (-44.096uV)/(\mu Inch)$$

$$\frac{d}{dR0}Udc = 1.21 \cdot N \cdot 10^{-12} \cdot fo^{2} \cdot 2 \cdot R0 = (3.525mV)/(\mu Inch)$$

The total change for a 0.05 AMU change is;

$$\Delta\mu Inch = \frac{(10V)/65536}{(44.096\mu V)/(\mu Inch)} = 3.460\mu Inches \quad \{ \text{RF voltage} \}$$

$$\Delta\mu Inch = \frac{(783.3915V)/65536}{(3.393mV)/(\mu Inch)} = 3.523\mu Inches \quad \{ \text{DC voltage} \}$$

To determine the ppm/C variance allowed is to know the amount of temperature variance of the quad. Since the quad is temperature controlled (indirectly), the assumption of 5C might be appropriate. Therefore, using the worst case number for the RF loop,

$$ppm/C = \frac{3.460\mu Inch}{0.4445Inch} \cdot \frac{(1\times10^{6})}{5C} = 1.557ppm/C$$

If the temperature can be held with 1C, then the ppm/C number is 7.785.

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REV	REVISIONS	APPROVED	DATE
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Bill Frazer DRAWN BY	04/21/97	**G1946-60002 Power Distribution Board Theory of Operation** TITLE	HEWLETT PACKARD
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SUPERSEDES DWG.	CURRENT REV A	PAGE 1 OF 9	**A-G1946-60002-5**

Overview: This document outlines the theory of operation behind the G1946-60002 power distribution board (PDB). This board resides within the Sprite electronics tub and mounts directly on top of the main power supply. It performs the following functions:

1)Power distribution and control. System voltages (+5, +/-15, +24, +28) are picked up from the main power supply and routed to the rest of the tub electronics. These voltages are routed through relays on the PDB that are interlocked with the top cover switch. Removing the top cover disables power to the tub electronics.

2)Temperature control. 120 VAC heaters (quad, drying gas, APCI vaporizer) are controlled by circuits on the PDB.

3)Flow Control. Proportional valves and pressure sensors on the flow manifold are controlled and monitored respectively by PDB circuitry.

4) CDS control and leak sense. The 24V calibrant delivery system valves, solvent selector valve, manual injector valve, and leak sensor are driven/sensed by PDB circuitry.

5) Misc. functions. Other PDB functionality includes driving and monitoring the speed of system fans, a real time clock (RTC) with 128 bytes of nonvolatile ram, RFPA power control and heatsink temperature monitor, and rough pump relay/system power led control. The PDB can also pull on the system shutdown line in the event of a vacuum failure.

The remainder of this document describes the above functionality.. The discussion treats each schematic sheet in detail by addressing the various components on each of the sheets.

Sheet 1-68332: The heart of the PDB is the Motorola 68332 microcontroller. This part contains a modified 68020 core with many useful peripheral functions 'on chip.' These functions include:

1) Chip select sub-module. This module virtually eliminates the need for external chip select glue logic. The 68332 can generate 10 external chip selects. On the PDB, the following chip selects are derived:

~CSBOOT/~CS_BOOT: Boot rom chip select (128k x 8 ROM)
~CS1/~CS_RTC: Real time clock chip select
~CS3/~CS_MISC: 8 bit latch for misc. control functions
~CS4/~CS_ADC_CH: 8 bit latch for analog multiplexor channel select
~CS5/~CS_ADC_CAL_SENSE: 8 bit tristate buffer for limit switches/misc. sensors.
~CS6/~CS_SOLENOID: 8 bit latch for controlling CDS solenoid valves
~CS7~CS_NEURON_LATCH: 8 bit tristate buffer for neuron communications
~CS8/~CS_LATCH: 8 bit latch used for neuron communications
~CS9/~CS_ADC: 12 bit ADC chip select
~CS10: 32k x 8 SRAM Chip select

2) Internal PLL clock generator. Using an internal PLL, the 68332 can generate its own 16MHz clock from an external 32.768kHz watch crystal. This significantly reduces radiated emissions from the part.

3) Time Processor Unit (TPU). This extremely powerful module consists of 16 separate i/o channels that can be configured in a number of ways. Some available options are pulse width modulation output, period measurement, interrupt generation with internal arbitration, and general purpose discrete i/o.

The 68332 is represented on the schematic as *U30*. The remaining parts on this sheet provide support functionality.

U13 is a TL7705B power supply supervisor. This part holds the 68332 in reset whenever VCC falls below the specified threshold (see engineering report for exact values).

U45 is a 74ABT541 octal tri-state buffer. It is used to drive various lines of the 68332's data bus during reset. Some of the 68332's internal functionality is set by the state of data bus lines as the part comes out of reset. Specifically, this buffer:

a) Pulls the MODCK line high on reset. This tells the 68332 to use its internal PLL to generate the system clock (as opposed to an external oscillator).
b) Pulls data bus line 0 (DB0) low on reset. This informs the 68332 that its boot rom is 8 bits wide.

U12 and *U29* comprise an 8 bit communications path with the LON Neuron chip. The 68332 writes to the Neuron via 8 bit latch U12, and reads data from the Neuron chip via U29, an 8 bit tri-state buffer.
U18 is a 128k x 8 flash eprom. It contains all of the program code for the 68332.

U33 is a 32k x 8 SRAM. Stack and program data are stored here. Note that the ROM and RAM are both 8 bits wide.

U19 is a mini-switcher. It generates the program voltage (+12V) required for erasing the flash memory (U18).

U3 is a 10MHz external clock oscillator. It is currently specified as a no load and in not used in this design.

Y1, C129, C130, R113,R114,R112 comprise the 32.768kHz oscillator circuit. The 68332 uses these components to generate a 32kHz signal that it then steps up internally to 16MHz.

J3,J3,J5 are logic analyzer pod connectors.

R74, R75, R60 are 22 ohm resistor networks. These resistors sit in line with the address bus. Their purpose is to dampen any ringing on the lines and improve system emi/noise performance.

Sheet2-Neuron: The PDB communicates with the rest of the Sprite system via the LON communications subsystem. This protocol requires the use of a special processor called a *neuron*. The neuron communications processor is basically an 8 bit microcontroller with a built in communications port that supports the LONTalk protocol.

U21 is a 3150 neuron chip. It sits between the LON bus and 68332 and passes data back and forth (temperature and flow setpoints/readbacks, diagnostic information, etc.). The neuron communicates with the 68332 via a simple 8 bit interface. The remaining parts on sheet 2 provide support for the 3150:

U5 is a TL7705B power supply supervisor. It holds the 3150 in reset until VCC rises above 4.2 volts.

U15 is a 10MHz oscillator used to clock the 3150.

U34 is an LTC485. This part generates the differential signals required for Sprite's RS485 (622kbit) implementation of the LONtalk protocol.

U6 contains program ROM for the 3150.

U30 and *U20* comprise a simple 8 bit interface to the 68332. Writes to the 68332 are latched by U30; reads are buffered by 8 bit tri-state buffer U20.

J2 is an 8 pin RJ45 shielded connector. Power and communication signals to the rest of the LON subsystem are routed through this connector.

J1 is no-load connector for a neuron emulator connection (RS232 signals to the 68332 are also available through this connector.

Sheet 3-ANALOG: Sheet 3 of the schematic contains most of the PDB's analog signal conditioning circuits. These circuits are used to bias, buffer, and scale signals from the various sensors interfaced to the PDB. These signals are selected via analog mux and routed into a 12 bit ADC that is read by the 68332.

U31 is a 706 dual precision pop-amp used to buffer pressure sensor output voltages. These sensors put out a 1-6V signal proportional to pressure (1V=0psig, 6v=100psig). This signal is halved (to accommodate the 0-5V range of the ADC) and then buffered before being routed to the analog mux.

U22 is also a 706 op amp. It currently has the potential to serve 2 functions. Its primary purpose is to serve as the leak detector signal conditioner. The leak sensor resides on the calibrant delivery board (G1946-60012) and is comprised of 2 hermetically sealed thermistors. One sensor is placed in the leak path, the other is in close thermal proximity but out of the leak path. A 5 volt regulator drives the 2 sensors in series and the midpoint voltage is sampled by the ADC. When a leak occurs, one of the thermistors becomes submerged in fluid. The fluid acts as a thermal conductor and reduces the temperature and hence resistance of that thermistor. This results in a change in the midpoint voltage. The 68332 measures the variation in the midpoint voltage and flags a leak fault. U22 is also wired to support an additional pressure sensor, but this feature is currently un-implemented.

U16 is another 706 dual op amp. The first op amp is used to bias RTD A (drying gas temperature sensor) with 2.5mA of DC current. The next op amp scales and levels this signal to match the voltage input range of the ADC. *CR13* and *CR11* are transient suppressor diodes used to protect the op amps from external transients (ESD).

U10 performs exactly as U16 above on the Quad Heater RTD.

U32 biases and levels the RFPA heat sink RTD. This RTD allows the 68332 to monitor the temperature of the RFPA heat sink.

U2 is used in the thermocouple amplifier circuit. Low level voltages from the APCI vaporizer thermocouple are often swamped by 60Hz common mode that couples over from the heater wires. To eliminate this coupled noise, a common mode rejection amplifier sits on the input of the thermocouple amp. To further reduce any residual 60Hz, a twin-T notch filter sits on the output of the thermocouple amplifier. U2 is used in the common mode rejection amp and also to buffer the output of the thermocouple network.

U1 is an Analog Devices thermocouple amplifier. It boosts the low level thermocouple signal into the 0-5V range of the ADC. It also linearizes the voltage and performs cold junction compensation.

U23 is used as an 'active clamp.' The ADC has a 0-5V input voltage range. The active clamps ensures that signals out of the analog mux are clipped if necessary to protect the ADC from over or under voltage.

U8 is an 8 channel analog mux. Select lines from 8 bit latch U9 select the active analog channel.

U9 is an 8 bit latch that sits on 68332's data bus. The 68332 selects an analog channel for A to D conversion by writing to this latch. Note that only 3 of the 8 available lines are utilized.

U14 is a dual comparator. This comparator is used to test the integrity of signals leaving the analog mux. For example, if the mux is set to channel 3, the ADC would ideally be monitoring the temperature of the drying gas. If a user forgot to connect the cable from the PDB to the drying gas heater, however, there would be an open circuit on U16's feedback path. The net result would be +15V out of the drying gas RTD circuit. This +15V would then be chopped to +5V by the active clamp circuit. The ADC would then send 4095 to the 68332. Normally, the 68332 would interpret this as +400C. By monitoring the outputs of the U14 comparators, however, the 68332 will see that the “~RTD_OPEN” line is active and it can then flag an error.

U25 is a 1.843MHz clock oscillator used to clock the ADC.

U24 is a 12 bit ADC. Conversions and data reads are initiated by the 68332. The ADC has a 0-5V input range and requires an external clock and reference.

U7 is a precision 5V reference used by several of the bias circuits and the ADC.

Sheet 4-Drivers. Most of the connectors that route signals and power to the rest of the Sprite system are located on sheet 4

P5 is the vaporizer heater connector. 120VAC (rms) for the heater, the thermocouple lines, and a 2 wire interlock are routed through this connector. When the interlock lines are open circuited, the 68332 disables power to the APCI heater.

P12 is used to connect to the primary power module (PPM). Drive signals for the system power LED and rough pump relay are routed through P12. The LED and relay reside within the PPM.

P7 provides drying gas heater connectivity. This DB9 connector routes lines for both 120VAC heater power and RTD signals.

P6 is used by the gas flow manifold. Connections to the drying gas and nebulizer proportional valves and pressure sensors are made through this connector. The pressure sensors are powered by +15V and return a voltage proportional to pressure.

P11 takes 120VAC from the isolation/step down transformer. This 120 AC voltage is used to power the drying gas, quadrupole, and APCI vaporizer heaters. Over-voltage protection is provided by MOV *RV1* and over-current protection is provided by a 6.3A fuse, *CB1*.

P4 provides a connection for a spare flow zone. This feature is currently unused.

P13 and *P8* are fan connectors. These +24V fans return a voltage wave-form proportional to rotation. This signal allows the 68332 to determine fan rpm.

P9 is used for RFPA power. +28V and remote sense lines are routed along with 2 lines for the rfpa RTD.

J6 is the adaptor board connection. Power to the rest of the Sprite tub electronics is sent through this connector. Also, the quad RTD and shutdown line are routed through J6.

P14 is a 96 pin Euro-DIN connector that plugs into the main electronics power supply. +5V, +/-15V, +24V, +28V, +28V remote sense, and all of the associated returns go through this connector.

P15 is a 3 pin AMP mate+lock connector used to route power to the QUAD heater.

U37 is a TL072 op amp. It is used here to buffer the 120V level signal. A voltage divider (*R94/R97*) steps the AC down to a manageable level. The reduced signal is then detected by *CR15/C80*. U37 buffers this voltage before it is routed to the analog mux on sheet 3-ANALOG.

U53 is an open collector output comparator. It is used to generate a “squared up” version of the 120V 60Hz. This square wave is then used to generate a 60Hz interrupt on the 68332 that is in sync with the line voltage. This interrupt allows the 68332 to switch heaters on or off during the AC voltage zero crossing (increases part life expectancy and reduces radiated/conducted emissions).

U11 is a 74ALS1035 open collector driver. It currently serves 2 purposes:

Pulls on the system shutdown line. The Neuron informs the 68332 whenever a vacuum fault occurs (high vacuum ion gauge turns off). In the event of a vacuum fault, the 68332 pulls the shutdown line low; disabling all system high voltages.

The 1035 is also used to drive the heater solid state relays (SSRs).

U36, U56, and *U26* are Aromat 5 amp solid state relays. They are used to drive the various 120V AC heaters. These parts are internally optically isolated and are configured as high side switches.

CR55 and *CR56* ensure minimum excursion between DCOM and ACOM. These lines should be tied together on the Sprite mother board; CR55 and CR56 are present to protect the PDB should it be powered up without that connection in place.

Sheet 5-FETS: As its name implies, sheet 5 contains many FETS used to switch relays and solenoid valves. This sheet also contains the stepper motor drive circuit, CDS step down switcher, and fan/power supply monitor circuits.

U57 (SHOULD HAVE A Q REF DES) is a FET used to implement the top cover interlock. The relays on its drain are used to gate power to the rest of the sprite electronics. When the top cover of the Sprite electronics tub is removed, these relays are opened; thereby cutting power to the rest of the electronics. Note, however, that the PDB and vacuum system remain live.

Q13 is used to gate the +28V to the rfpa. Power to the rfpa is enabled by the 68332. The 68332 will cut power to the rfpa whenever the top cover is removed, or if an 'overheat' condition is detected through the rfpa heatsink RTD.

Q14 is used to control the 120V relay. This relay is provided for thermal runaway protection. It can be opened by the 68332, and also indirectly by the 3150 neuron (the 3150 can hold the 68332 in reset if it detects communications errors).

Q12 is used to drive the rough pump relay. This relay is located within the primary power module.

CR43 is a transient suppressor diode used to provide both transient and flyback protection to Q12.

Q11 drives the system power LED; also located within the primary power module.

Q4,Q5,Q7,Q8,Q9 are used to drive the calibrant deliver system (CDS) solenoid valves. The diodes on the drains of these FETS are transient suppressors that provide both ESD and flyback protection.

U49 is an 8 bit latch. This latch is written to by the 68332 to turn the CDS solenoids on or off. The two higher order bits are used to enable the CDS step down switcher and stepper motor drive respectively.

U48 is a switching regulator wired in a step down configuration. The CDS solenoids require 24V initially to open. After a short turn on period, however, this 24V can be reduced to 10V or so. Reducing the voltage across an open solenoid saves power and reduces thermal stress on the valve. The step down switcher generates this solenoid hold voltage. When a valve is to be opened, the 68332 sets bit 7 of U49. This disables the switcher and puts the full 24V across the CDS valves. The 68332

then enables the appropriate FETS by writing to U49. After a short delay, the 68332 clears bit 7 of U49. This enables the switcher; which then reduces the solenoid voltages to 8.5V. Note that the supply voltage is common to all solenoid valves.

Q6 is used to enable/disable the CDS switcher. When turned on, Q6 pulls the feedback line of the switcher to ground. This causes the switcher to turn full on and effectively pass 24V to the solenoids.

U51, U54, and *U55* comprise the stepper motor drive circuit. This circuit is used to drive the solvent selector valve (SSV) stepper motor. The coil wave-forms are generated by the 68332's TPU. U51 is the control IC, U54 and U55 are full bridge drivers that drive 1 coil each. When moving the SSV, the 68332 first enables the stepper circuitry by writing to U49, bit 7. The stepper motor is then full-stepped until the appropriate limit switch closes. Note that the limit switches are constantly monitored. If a limit switch open is detected, the 68332 will immediately begin stepping the motor until switch closure occurs.

U52 is a quad comparator. It is used as a window comparator on both the 24 and 28 volt supplies.

U50 is an 8 bit tri-state buffer. It is used to buffer the window comparator outputs, the stepper motor limit switches, and the manual selector valve sensor switch.

J7 is a DB25 connector. The CDS solenoids, stepper motor, selector valve switch, stepper motor limit switches, and turbo fan are all routed to the CDS control PCA through J7.

CR28, CR29, and *CR30* are shottky diodes used in the fan speed sense circuits. The fans each contain an optical transistor that is cycled on and off as the fan rotates. Oddly enough, each fan is slightly different (one has a pull-up to 24V, the other has a zener/resistor pullup to 24V, and the third one is open collector); the shottky diode connection eliminates the effects of these output network differences. The sense wave-forms are routed into the 68332's TPU where the rotational speed of the fans is measured.

Sheet 6-MISC: Sheet 6 contains the flow control valve drive circuitry, a relay/misc. output latch, and the real time clock interface.

U44 is a hex inverter. It is used in the flow drive and cover interlock circuits.

Q1, Q2, and *Q3* are used to drive the flow system's proportional valves. These 24 volt proportional valves are used to control the flow of the drying gas and nebulizer. If a DC voltage (0-24V) is placed across one of these valves, an orifice within the valve will open. The higher the voltage, the larger the opening. Rather than use variable DC voltages to drive these valves, however, the PDB uses pulse width modulated (PWM) signals. Thus, 24 volt switching wave-forms are placed across the valves. The mechanical inertia of the valves is such that steady flow is obtained despite the switching nature of the drive. This PWM drive mechanism eliminates the need for a separate DAC for each flow zone and also reduces the power dissipated within the drive transistors. The PWM wave-forms are generated by the

68332's TPU. The signals are inverted through U44, their edges are 'rounded' and then they are run into the gates of Q1-Q3. *CR6*, *CR7* and *CR8* provide transient and flyback protection for the FETs.

U40 is a 74ACT138 3:8 decoder. This part is used to generate glue for the real time clock (RTC) interface. 2 selects are required by the RTC, and another chip select was required for U41. The 68332 had only one additional CS pin available, hence the use of discrete glue logic.

U39 is a quad 2 input nor gate. It is used for RTC glue.

U46 is an 8 bit latch that gates many of the relay interlock signals. This part is written to by the 68332.

U41 is a tri-state buffer used to gate diagnostic signals from sheet 3 to the 68332's data bus.

DL1 is a delay line used in the real time clock interface. The RTC requires that the DS line become active no sooner than 20nS after CS becomes active. The delay line implements this hold off.

U35 is a real time clock. This part contains a lithium battery good for 10 years of operation along with 128 bytes of non volatile ram and, of course, a clock. The bus interface for this part is a bit complex due to the multiplexing of address and data information onto the same 8 lines. In order for the 68332 to write or read from the RTC, it must first latch the internal address of interest. This is done by writing the 8 bit address to the part and toggling the AS line. The next data operation on the part will then affect data at the address previously latched. Data is written or read by clocking the CS and DS lines. Note, however, that DS must be delayed from CS; these signals cannot be coincident.

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Theory of Operation
G1946-60004-5

1.0 Introduction

The assembly, G1946-60004, is referred to as the Coil Driver board. Its main goal is to combine the RF and DC quad drive signals together to drive the RF Coils. The RF quad drive signal is a single ended AC signal coming from the RF Power Amplifier. This signal typically ranges from 0 to 120 volts peak-to-peak and runs at 1 Mhz. The DC quad drive signals are two DC voltages that range from 0 to 750 volts and 0 to -750 volts.

2.0 Schematics

There is only one schematic page for this assembly. The schematic is broken up into two functional areas; 1) the power coupler circuit, and 2) the coil drive circuit. The main goal of the power coupler is to provide two voltage signals that are proportional to the forward and reflected power delivered to the coils. The main goal of the coil drive circuit is to mix the AC and DC components together to drive the coils.

2.1 Power Coupler

The power coupler circuit measures the forward and reflected power on the RF signal based on the phase relationship of voltage and current. Connector P6 is a BNC connector that brings in the 1 Mhz AC signal from the power amplifier. Capacitors C6, C4 and C2, C3 voltage divide the incoming signal. The transformer T2 is a single turn primary used to generate a voltage on the secondary that is proportional to the current through the primary. The output of the secondaries are loaded by resistors R2 and R6. The diodes CR1 and CR2 couple the current and voltage measurements on to the load resistors R1, R3, R4 and R5. Filter capacitors C5 and C7 help remove the AC noise to create a DC voltage out of connector P7. One side of the coupler circuit provides the forward power and the other side provides the reflected power. The typical voltage levels versus power are shown on the schematic.

The forward and reflected measurements can be used to help determine the resonance of the coils with the quad. The quad should be driven at resonance in order to minimize the amount of power required to get to higher masses. When the coils and quad are at resonance, the load on the RF signal produced by transformer T1 is minimized and real, no phase angle. Looking in to the transformer T1, the impedance is approximately 50 Ohms at resonance. The amount of power to drive 50 Ohms is measured by the power coupler circuit. At resonance, the reflected power is minimal and all of the power into the coils is “forward” or delivered power.

2.2 Coil Drive

The coil drive circuit couples the AC and DC components of the quad drive signal together to drive the coils. Transformer T1 is the coupling transformer. This transformer has a 15:3 turns ratio with a split secondary. This turns ratio was determined experimentally to get 50 Ohms of impedance for the power amplifier at resonance. The secondaries are split in order to apply the DC components needed on the quad. The DC signals, U+ and U-, come in on connector P1. R7 and R8 add a little resistance to kill any self resonances that may develop. Between the split secondaries is a 1 Mhz resonant circuit. The goal is to achieve an AC short and a DC open. C8 and C9 are high voltage capacitors. Two capacitors are used to get 4400pF and to split the circulating current. L1 is a nominal 5.5uH variable inductor. The adjustment is done with an adjustment screw through the middle of the POT core. The adjustment is made to minimize the AC on the U+/U- signals. If too much AC is on the U+/U- lines, then non-linear settings occur in the U/V ratio. This causes non-linear peak widths and mass assignments. The connectors J1, J2, and J3 are single pin connectors that

connect the coils and the rf return line from the Doil Detector board, G1946-60005.

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Engineering Report
A-G1946-60004-6

1.0 Introduction

This document will describe details not discussed in the Theory of Operations document. There will be some notes on design decisions and reasons for designing the card.

2.0 Design Theory

The purpose of the assembly is to couple the AC and DC components needed to drive the coils and quad. This board gets its AC component from the power amplifier and its DC component from the Analyzer board. Since most commercially available power amplifiers are designed with an output impedance of 50 Ohms, it made sense to design the AC part of the board to resemble 50 Ohms at resonance. Furthermore, there can be up to 50 watts of power delivered to the coils which results in a lot of high voltage and high current. It made sense to put this assemble inside of the coil box to help shield the RF signal and protect users from high voltage.

3.0 Design Considerations

There were many areas of concern during the design of this assembly: 1) high circulating current, 2) power coupling voltage levels, 3) feedthru connections and 4) grounding. Each of these concerns played a major role in the design and layout of the board.

3.1 High Circulating Current

The coupling circuits are the same design topology as MS ENGINE. With SPRITE, the circulating current is 1/3 higher due to the higher mass range. This high circulating current caused the original variable inductor, L1, to get very hot. The original value was nominally 11uH. By reducing the number of turns and double winding with litz wire, this heating problem went away. We ended up with nominally 5.5uH. The capacitance was doubled to keep the LC product the same.

3.2 Power Coupling Voltage Levels

The power coupling circuit was originally taken from a design in YAN's ICP-MS. Their circuit was designed to measure power up to 150 watts running at 3 Mhz. The component values were changed to optimize a range of 50 watts running at 1 Mhz. This involved lowering the capacitance values of C2, C3, C4 and C6. Also, the load of the coupling circuit was minimized so as not to change the 50 Ohm load spec. of the RF Power Amplifier. C1, a small filter capacitor, is not loaded at this time.

Another problem that occurred early in the Pilot Run phase of the project had to do with the circuit on the Analyzer board that buffers the power monitor voltages from P7. When the cable was connected between P7 and the Analyzer board, the buffer opamp would blow. It seemed that a voltage spike would occur that would run out the cable to the Analyzer board. We think that the problem is due to arcs in the quad. We were never able to find the real cause of the problem or a fix, so we do not install the cable between the coil box and the Analyzer board. However, the buffer opamps on the Analyzer board have resistors and zener clamps added to minimize the arcing effects. In future designs, we should consider removing the power coupling circuit altogether. We are able to "dip" the quad by reading the RF DRIVE level from the Analyzer board.

3.3 Feedthru connections

The single pin connectors, J2 and J3, that are used to connect to the coils are not the best parts. These connectors can work, but they start to degrade after plugging and unplugging the mating connector several times. Future design changes should consider changing to a better part. We currently solder the mated connectors.

3.4 Grounding

All of the grounds on this board are tied to the RF Power Amplifier ground at the BNC connection. The U+/U- ground reference is not tied to this board since it might cause a ground loop relative to the RF Power Amplifier. Furthermore, the shroud of the quad is tied to the BNC ground. We thought that this seems like the most appropriate point to ground the shroud since any AC unbalance in the quad would pump the shroud. This pumping current should return to the source which is the ground of the RFPA.

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Theory of Operation
A-G1946-60005-5

1.0 Introduction

The assembly, G1946-60005, is referred to as the Coil Detect board. The main goal of this assembly is to detect the RF voltage applied to the quad from the coils. The RF voltage is a 1Mhz, 0 to ~4200 volt peak signal generated within the coil box assembly and applied through two feedthrus to the SPRITE Quad. The voltage is sampled by a high voltage capacitor, rectified, and filtered to provide an average current proportional to the peak voltage. The average current is then fed into a closed loop control system to accurately set and maintain a given voltage on the Quad.

2.0 Schematics

There is only one schematic page for this assembly. The schematic is broken up into two main sections; 1) the heaters, and 2) the detect circuit. The main goal of the heaters is to maintain a constant temperature on the sampling capacitors to minimize any T_c effects. They also try to keep the whole assembly, including diodes, from drifting too much in temperature. The main goal of the detect circuit is to sample the RF voltage and generate an average current that is sent to the Analyzer board, G1946-60001, through the connector J1.

2.1 Heaters

There are four zones in the heater circuit labelled zone A through zone D. Four zones where chosen because the sampling capacitor had four mounting screws to heat and four zones provided ample heat without over driving the transistors. Each zone operates exactly the same. Since the instrument is tested to 40^{o}C, the set point of the heater must be above 40^{o}C and is set to approximately 45 to 50^{o}C.

The first part of the heater design is the bridge network setup by resistors R45, R46, R47, R26-R29, and RT1-RT4. The bridge network is biased between ACOM and -15V. ACOM is not only the ground of the circuit, but it is the copper area that heats the sampling capacitor. Figure 1 is a simplified diagram of the bridge circuit.

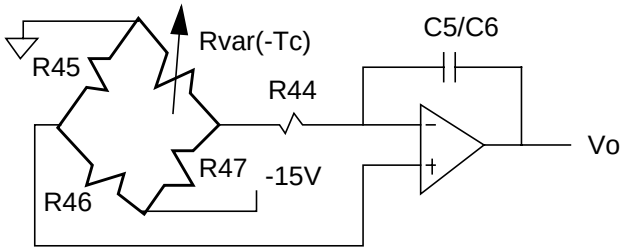

Figure 1. Bridge Circuit

The bridge circuit is biased at -7.5v by resistors R45 and R46. This bias is half way between the bias of the opamp, U1, and the heaters. This allows for operation of the heater design over the largest range. Rvar in Figure 1 is a combination of RT1-RT4 and R26-R29. When Rvar equals R47, then the integrator stops integrating and a balance point

is met. As the board heats up, Rvar becomes smaller which makes Vo less. Each RT resistor is weighted with a series resistor (for example, RT1 with R28) to provide a “gain” of the temperature resistive device. The time constant of the integrator is very long because of the thermal time constant of the heaters and the temperature sensors.

The voltage out of the integrator is sent as a set point to the four heater zones. Zone A takes the voltage directly and the other three zones buffer the voltage with the spare opamps in U1. Using heater zone A as an example, the heater is a biased power transistor, Q1, that simply generates heat by dissipating power out the collector. The collector of the transistor is tied to ACOM which is common to the sampling capacitor. The set point voltage is first dropped by a zener diode, CR3. This helps keep the integrator near the center of the bias voltage during normal operation. Following the zener diode are two resistors. The first resistor, R36 provides some base resistance to the transistor. The second resistor, R39 is used to guarantee that the power transistor is off when the integrator drives to a lower voltage (pull down resistor). The resistors R21, R22, and R23 are emitter resistors. They keep the transistor biased properly and also set the “heat” gain of the transistor. The smaller the resistance, the higher the gain of the transistor. There are three resistors used to help dissipate the current through the emitter. The other zones operate exactly the same.

2.2 Detect & Compensation Circuits

The detect circuit is made up of the sampling capacitor, detection diodes, and some temperature sensor devices. The goal of the circuit is to sample both phases of the RF signal that drives the quad. The amplitude of a 1 Mhz sinusoidal signal at 3200 AMU using the SPRITE quad is approximately 4565 volts peak. The sampling capacitor is a custom made dual capacitor design encased in a metal block. The through capacitance is approximately 1.1pf and the guard capacitance (capacitance from the input pin to the metal block) is approximately 5pf. The metal block is the element that is heated by the heater zones. If it is kept at a constant temperature, then the T_c of the capacitance is minimized. The detect diodes, CR5 and CR6, are used to rectify the RF signal coming through the sampling capacitor. The rectified signal is then filtered by C4 and sent out the connector J1. The current through the diodes is proportional to the mass setting. The following table shows some of the current requirements for the diodes.

Table 1: Typical Voltage/Current of Detect Circuit

Mass [AMU]	Vpeak	Iav	Imax
500	713V	3.14mA	4.93mA
1000	1427V	6.28mA	9.86mA
2000	2853V	12.55mA	19.72mA
3000	4280V	18.83mA	29.58mA
3276.75	4674V	20.57mA	32.31mA

The diode CR7 is used to sample the temperature of the detect diodes and compensate for any voltage drops from the detect diodes. The temperature sensor, RT5 is used to sense the temperature of the sampling capacitor and compensate for any changes in temperature.

2.3 Miscellaneous

There are a few miscellaneous parts on the board. P1, P2 and P3 are single pin connectors that connect to the

feedthrus on the vacuum manifold. The pins pass on the two high voltage quad drive signals and the RF ground return signal. J2, J3, J4, and J5 are signal pin connectors for attaching the high voltage coils and the leads to the sampling capacitor. J6 is a single pin connector for connecting a ground lead from the driver board, G1946-60004. This lead provides the RF ground return back to the common ground of the RF Power Amplifier. Resistors R42 and R43 are in series with the ground return to kill the "Q" of any resonances that may develop from the shroud. In general, there should be virtually no current in the ground return. If current exists, then there is an unbalance in the two phases of the quad.

3.0 Layout considerations

The main focus in layout was to create a good heat conductor from the heater zones to the sampling capacitor. Each heater was placed near the mounting screw of the sampling capacitor and a larger copper fill was generated to help minimize heat impedance. Also, the temperature sensors were place in the copper fill so that they could sense the heat accurately. The temperature sensor, RT5, is placed in a slot of the sampling capacitor to accurately sense the cap's temperature.

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Engineering Report
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1.0 Introduction

This document will describe details not discussed in the Theory of Operations document. There will be some notes on design decisions and reasons for designing the card.

2.0 Design Theory

The purpose of the card was to provide an easy method of connecting the high voltage coils to the quad feedthrus and to attach the samping capacitor. The whole concept revolved around the coil box assembly that holds the high voltage coils, the RF Driver board, and the Coil Detect board. These items are held together by HP-PAC inside of a metal container. The HP-PAC does an excellent job of holding the board in place and it also provide some thermal insulation to help the heater zones for heating the sampling capacitor. Also, all high voltages are protected from the outside since the only signal coming out of the box is the sampled current from the sampling capacitor and rectifying diodes.

Another area of design that was considered was the relationship of the quad capacitance with the coil inductance. On the MS ENGINE design, the coils and detect circuit were a considerable distance away from the quad feedthrus. Therefore, the instrument needed high voltage cabling that ran from the RF DRIVER assembly to the manifold. These cables were heavily insulated to protect people when the covers were off the instrument. These cables provided a certain amount of variable capacitance that increased the overall capacitance of the quad as seen from the coils. Therefore, the inductance of the coils on SPRITE had to be increased in order to resonate at 1 Mhz. It was in our best interest to minimize capacitance seen from the coils in order to minimize the amount of drive to get to 3000 AMU.

3.0 Design Considerations

There were many areas of concern during the design of this assembly: 1) high voltage, 2) temperature control, 3) feedthru connections and 4) detection circuit. Each of these concerns played a major role in the design and layout of the board.

3.1 High Voltage

One of the major design goals was to keep all high voltages hidden from users. The coil box design keeps all of the high voltages contained. The Coil Detect board keeps the lead lengths very short in going from the coils to the quad feedthrus. This greatly minimized the overall capacitance such that the number of turns on the coils increased by at least 16 turns. This actually helped increase the “Q” of the resonant tank circuit and minimized the amount of power needed to get to 3000 AMU.

3.2 Temperature Control

As described in the Theory of Operation, the sampling capacitor is heated and controlled to minimize temperature drift. The layout has a big effect on the performance of the heater zones. The layout has to have very good thermal contract with the sampling capacitor. Large copper fills were added at the mounting holes, and the RTD was placed in the copper fill fairly close to the heater. One thing noticed with the design is that the temperature sensor is mainly sensing the heater and not the sampling capacitor. The closer the sensor is to the sampling capacitor, the better the sense is of the

capacitor. However, the time constant of the integrator might have to change to compensate for the increased thermal delay.

Another area of concern with the heated zones is the thermal loss to air. The coil box PAC is designed to make an insulated section for the coil detect board. This works pretty well in that the air blowing across the coils does not blow across the samping capacitor. Air flow across the capacitor could greatly affect the capacitance of the device which causes peak position and peak width errors.

3.3 Feedthru connections

One of the drawbacks of this design is the single pin connectors used to connect to the quad feedthrus. Early on in the SPRITE project, the quad feedthru wire was 50 mil thick which required a contact of equal value. This contact had reasonable margin for passing on the high voltage, but mainly carrying the high circulating current which is approximately 6.5A peak at 3000 AMU. The quad feedthrus later changed to 40 mil which required a smaller single pin contact. The smaller contact will work, but it starts to fail over time if the coil box is removed and inserted many times. Any design changes should consider changing to a better single pin contact.

3.4 Detection Circuit

During the design of this board, we played around with the detection circuit to see what affect the filter stage following the rectifying diodes had on the design. We found many problems with the filter stage which eventually pointed to the inductor used to filter the current. In a normal environment, the inductor with a capacitor will act like a second order low pass filter. Our goal was to filter the 1Mhz rectified signal to a DC current. It turned out that having a filter inductor inside of the coil box causes many problems. The magnetic field is very strong inside the box. This magnetic field would simply couple directly into the inductor coil which would then pass right out to the detection circuit opamp on the analyzer board. This caused noisy peaks and non-linear effects. We concluded that there should never be any inductors in the coil box. Therefore, the first capacitor of the filter stage is the only element inside of the coil box. The inductor and all other elements are on the Analyzer board.

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REV	REVISIONS	APPROVED	DATE
A	AS ISSUED PER PC23-6030	N. MOREYRA	3/10/98
B	Changed MRF137 to the BLF145 per EC23-70201	B. CAPRILES	1/5/99

Overview: This document describes the theory of operation behind the G1946-60006 radio frequency power amplifier (rfpa). This part is capable of generating 60 watts of output power at 1MHz into a 50 ohm load. It is used in the G1946A (Sprite) mass spectrometer to generated the AC voltages required by the quadrupole mass filter. This document consists of 2 parts. Part I discusses the operation of the rfpa. Part II provides a detailed description of the design on a part by part basis.

Operation. The principles behind the operation of the G1946-60006 rfpa are fairly straight forward. The rfpa takes a low level, variable amplitude 1MHz waveform as input and provides a greatly amplified version of that waveform as output. The rfpa receives its input from the analyzer board (G1946-60001). The rfpa's output is routed to the coil box where it stimulates a resonant LC circuit. +28V power for the rfpa comes from the power distribution board (PDB, G1946-60002).

The resonant LC circuit within the coil box provides a great deal of voltage gain. It steps the 56V (peak to peak) output of the rfpa up to thousands of volts. In order to maintain this voltage, losses within the resonant tank must be compensated for. The primary purpose of the rfpa is to provide the necessary power to overcome these losses (typically ~30W at 3000 amu).

Generating 60 watts of output power at 1MHz is a nontrivial matter. Special transistors are used that are capable of developing large amounts of power. To ensure acceptable efficiency and long term reliability, a great deal of attention must be paid to transistor input/output impedance matching and heat dissipation. The rfpa addresses efficiency by using specially wound matching transformers. To ensure proper heat dissipation, a very large heat sink is used. The rf transistors come in a special package that affords extremely close thermal contact with the heat sink. A block diagram of the rfpa is provided in figure #1.

Power amplification in the rfpa is performed by 2 cascaded stages. Stage one performs initial amplification of the input signal. The output of this stage is fed to a class AB output stage. A transformer between stages 1 and 2 acts to split the stage 1 output waveform into 2 out of phase waveforms for use by the second stage transistors.

Most of the rfpa's output power is developed in the second/output stage. The output stage consists of 2 transistors, each of which amplifies a half cycle of the 1MHz waveform. The output of the second stage passes through another transformer that matches the output impedances of the drive transistors to the load (50 ohm nominal). Matching the output impedance of the transistors to the load ensures that the transistors can generate maximum power into the load.

This transformer also takes the two 'out of phase' waveforms generated by the output transistors and combines them into a single sinusoid. The output waveform is next passed through a second order low pass filter (for har-

monic attenuation) and is then routed to the coil box.

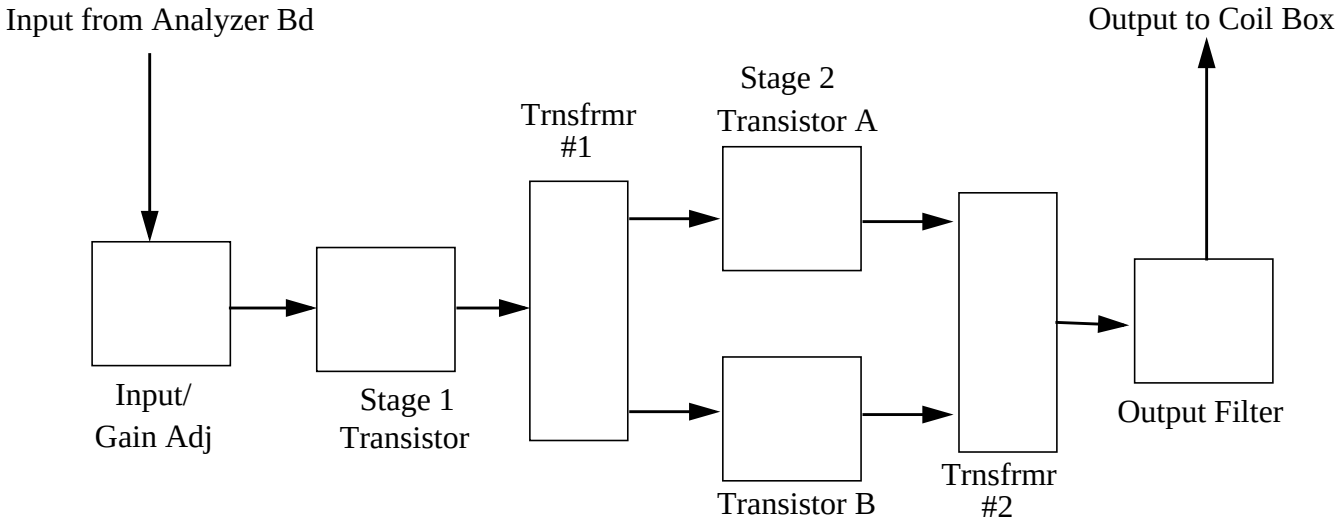

Figure 1
RFPA Block Diagram

The rfpa is actually a fairly simple circuit. Refer to the attached schematic (C-G1946-60006-1). As is evident, the function of most components is fairly obvious. Transformers #1 and #2, however, deserve special note. The following paragraphs attempt to clarify the operation of these 2 critical components.

Transformer #1 (refer to figure #1) splits the output from stage 1 into two out of phase components. This transformer is specially wound to reduce the effects of leakage inductance. Leakage inductance can cause major headaches in high power/high frequency circuits. It can make an otherwise solid design unstable and/or inefficient.

Leakage inductance is caused by the incomplete coupling of flux between separate windings. Leakage inductance is modeled by placing inductance in series with the transformer winding. If the transformer is being driven from a low impedance amplifying element (e.g. a power transistor), this series inductance can severely hamper the transistor's ability to deliver high power to a load (the impedance of the series inductance reduces the magnitude of the output current). +28V power transistors have extremely low output impedances (~5 ohms). To deliver maximum power, these transistors should drive a load whose impedance is equal to their output impedance. Thus parasitic impedances of only a few ohm will severely limit the drive capability of the circuit. Figure #2 illustrates the effects of leakage inductance. Two transformer models are depicted. The first transformer has no leakage inductance. The second models leakage inductance by placing a small inductor in series with the primary winding. The net impedances of the network are quite different. The impendance difference would have a significant impact on the amount of real power delivered to the load when those networks are driven from a low impedance source.

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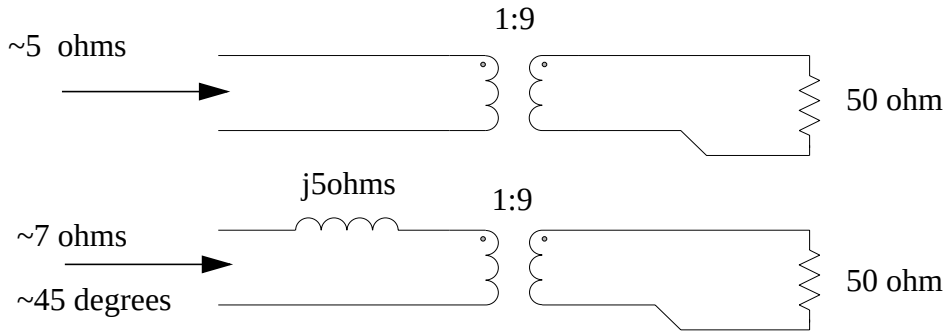

Figure #2
Leakage
Inductance

The winding strategy of transformer #1 is geared to reduce leakage inductance. It is bi-filar wound; meaning that 2 wires are first twisted together, and the resultant twisted pair is wrapped around the ferrite core.

The following paragraphs attempt to outline the operation of this bifilar transformer. It is shown that the transformer provides low leakage and impedance transformation. To understand the operation of this transformer, examine figure #3

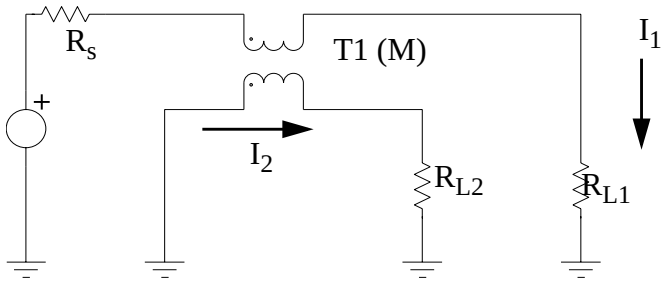

Figure #3

A voltage source feeds the transformer through its internal source resistance R_s. R_{L1} and R_{L2} represent 2 load impedances. The following analysis assumes:
1) Both winding of the transformer have the same impedance
2) The coupling coefficient of the transformer is very close to unity
3) Load impedances R_{L2} and R_{L1} are equal

Using KVL on the upper loop (steady state frequency analysis is assumed) yields:

$$Vs = R_s \times I_1 + Z_{T1} \times I_1 + Z_m \times I_2 + R_L \times I_1 \qquad \text{Eq \#1}$$

Where Z_{T1} is the impedance of the primary winding of T1 and Z_m is the effective impedance given by the mutual inductance of the transformer. I_1 is the current flowing in the top winding. I_2 is the current flowing in the bottom winding. Another equation can be written for the lower loop:

$$0 = Z_{T1} \times I_2 + Z_m \times I_1 + R_L \times I_2 \qquad \text{Eq \#2}$$

This yields 2 equations in two unknowns (I_1 and I_2). Solving for I_1 and I_2 yields:

$$\frac{V_s}{R_s + Z_{T1} + R_L - \frac{{Z_m}^2}{Z_{T1} + R_L}} = I_1 \qquad \text{Eq \#3}$$

And

$$I_2 = -I_1 \times \frac{Z_m}{Z_{T1} + R_L} \qquad \text{Eq \#4}$$

Equation $4 yields some immediate results. If we want to split the output power from the voltage source equally between the 2 loads ($|I_1| = |I_2|$) then Z_m and Z_{T1} should be large compared to R_L. Also, Z_m and Z_{T1} should be very close in net impedance (this is ensured if the coefficient of coupling is close to unity).

Some not so obvious results are obtained through further examination of the solution to Eq #3. It turns out that with proper selection of Z_{T1} and Z_m for the given R_L, we can also obtain an impedance transformation with this transformer. An analog simulation of the network found in figure #3 is used to illustrate the concepts::

Figure 4. Simulation Output

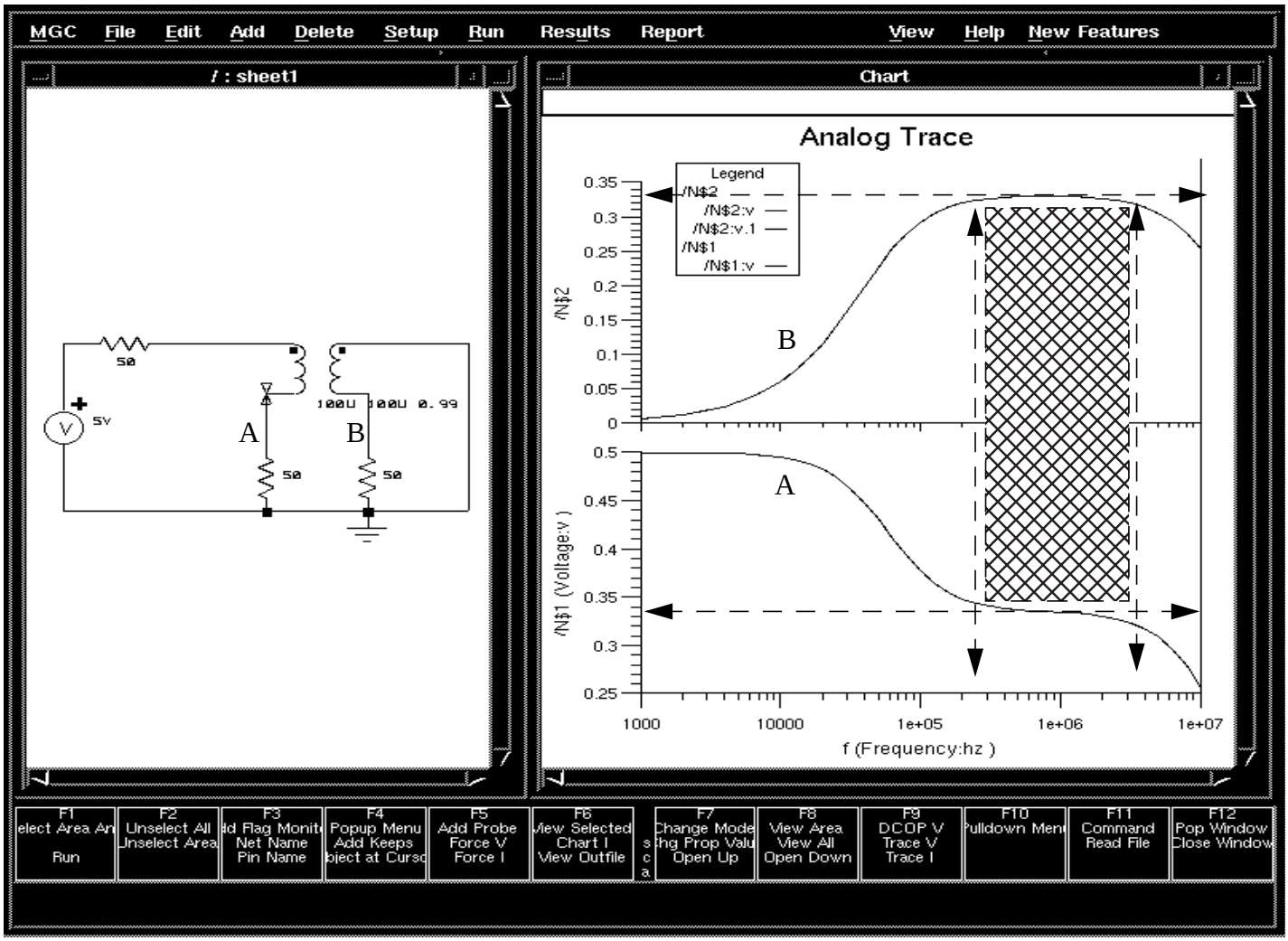

Figure #4 is the output of a simulation using the circuit from figure #3. Traces A and B represent the voltage on each of the load resistors versus frequency. The shaded area of the plot represents the point at which the voltages at points A and B are the same (an equal power split is occurring). Note the magnitude (~0.32) of the voltage at A and B in that region (the voltage source has unity magnitude).

$$0.32 volts = R_L \times |I_1|$$

$$R_L = 50 ohm$$

$$|I_1| = 0.32/50 = 6.4 mA$$

Thus. 6.4mA is being drawn from the voltage source. Let R_{eff} be the effective impedance seen by the source:

$$R_{eff} = \frac{Vs}{I1} = 1/0.0064 \sim 150 ohms$$

This 150 ohms is the net impedance of the circuit as seen from the source. It consists of 50 ohms of source impedance in series with the net impedance of the transformer circuit. The 50 ohm R_L impedance has been 'transformed' into an effective 100 ohms of impedance. The transformer has performed a 2:1 impedance transformation. Note, that as long as various criteria on Z_{T1} and Z_m are met, this transformed impedance is real (the source voltage's output current is almost totally in phase with the source voltage).

The above discussion is intended to illustrate the concepts behind the multi-filar wound transformer. It acts as both a power splitter and matching element. The twisted nature of the winding ensures that almost all flux is coupled from one winding to the other. This dramatically reduces the net leakage inductance; a critical parameter in the rfpa circuit transformers. Another point to observe is that by using 2 windings of equal length, the "manufactureability" is improved. One need only wrap twisted pair wire around a ferrite core (coaxial wire would also work well). Compare this to a conventionally wound transformer that performs impedance transformation. Such a transformer would require separate windings of different lengths. It would be very difficult (and expensive) to make such a transformer with high impedance windings and minimal leakage inductance.

Transformer #2 (figure #1) also deserves special note. This part is responsible for matching the relatively high impedance of the load (50 ohm) to the low output impedances of the drive transistors (~5 ohms). It also combines the output of the two transistors into a single sinusoid. This part consists of 3 wires in a tri-filar arrangement. In this case, 3 wires are first interleaved to form a 'twisted 3'' that is then wrapped around a ferrite core. The concepts behind this transformer are the same as those outlined above for transformer #1. In this case, however, a 1:9 impedance transformation is obtained. This allows the low impedance power transistors to drive the relatively high impedance load (the 50 ohm load is transformed down to ~5-6 ohms).

Design Discussion. The remainder of this discussion focuses on the RFPA schematic (C-G1946-60006-1) For the most part, this schematic correlates with the rfpa block diagram (figure #2) quite well. The following paragraphs outline the purpose of each component on the schematic on a part by part basis.

P1. This is an SMB input connector. The modulator output (low level 1MHz) is routed from the analyzer board to the rfpa through this connector.

R2: This potentiometer is used to adjust the overall gain of the rf loop. Ideally, the output of the rf modulator on the analyzer board should be 85% when driving to 3000amu. This potentiometer is used to adjust the gain of the loop to compensate for tolerance variations in the various components that comprise it.

R1: This series 10 ohm resistor provides a pad for further attenuation of the rf loop. On previous versions of the rfpa, this resistor was set to 100 ohms but was later changed to 10 ohms. It could be omitted entirely, but it was felt that the pads should be maintained in order to accommodate any future changes that may modify the overall loop gain.

R19. This 51.1 ohm resistor is placed in parallel with the input stage of the rfpa. Its purpose is to effectively

swamp out the input capacitance of the stage one transistor. If this capacitance were uncompensated, it would cause the rf loop to dip slightly off resonance.

C9. This capacitor provides DC isolation between the stage one transistor's bias circuitry and the rf modulator.

R20: This 51.1 ohm was added to eliminate high frequency oscillations (400MHz+) observed on the stage one transistor.

R7: This 1k ohm resistor feeds the DC bias voltage to the stage 1 transistor.

C31 and C33 provide bypass for the input of the 15V linear regulator.

U1: This 3 terminal linear regulator provides a clean +15V from the +28V for use by the transistor bias circuits.

C32 and C34 bypass the output of the +15V regulator.

R9 and R10: This series resistor/poteniometer combination is used to generate the DC bias for the stage one transistor. During rfpa bench test, pot R10 is adjusted such that 0.25 amps of bias current is established in the stage one transistor.

C23 provides bypass for the stage one transistor voltage.

C3 and C4 provide bypass for the +28V.

L1 acts to filter the stage one drain circuit.

C14 and C15 provide further filtering on the stage one drain circuit.

T1. The secondary of this transformer is left open. It is used in the stage one drain circuit as an rf choke.

Q1 is the stage one transistor. This part provides initial amplification of the input signal.

R15. This 10 ohm power resistor stabilizes the gain of the input transistor amplifier circuit.

C27 acts to block the +28V on Q1's drain from its load (transformer T2).

T2: This transformer couples the output of Q1 to the input's of the stage 2 transistors. See section 1 of this document for a more detailed description of T2's operation.

R5 and C16/R8 and C17: These networks attenuate the signal from the stage 1 transistor at very high frequencies.

C11 and R4 / C28 and R11 provide a minimum real load for the stage one circuit. They help stabilize the circuit.

L4 and C41/ L5 and C42. These resonant networks provide low frequency power supply noise rejection. The +28V supply that powers the rfpa exhibits a significant amount of low frequency (<10kHz) noise. On previous revisions of the rfpa, this noise sometimes propagated through the low impedance neutralization (feedback) networks (R3 and R6) and wound up on the gates of the stage 2 transistors. The noise was then amplified and passed on to the rf tank. The result was unstable spectral peaks. These resonant networks provide low impedance at low frequencies (shunting the supply noise to ground) and high impedance at the rfpa's frequency of operation (1MHz).

R3 and C5|C6|C10 / R6 and C21|C24|C25: These components form "neutralization" networks. This is just a fancy way of saying they provide negative feedback to ensure the stable operation of the stage 2 transistors.

R12, R13, R16, C35 and R17, R18, R14 and C36 comprise the stage 2 transistor dc bias networks. During rfpa bench test, poteniometers R16 and R18 are adjusted such that 0.5A of bias current is developed in each transistor.

Q2 and Q3 are Philips BLF145 high frequency MOSFET's. These parts develop all of the output power for the rfpa. Each transistor is responsible for amplifying approximately a 1/2 cycle of the input waveform. These parts are rated at 30Watts max output power for a total of 60 watts available output power. Special packaging ensures close thermal contact with the heat sink.

C12, C13, and C18 are all no-loads. The pads have been retained to accommodate any future modifications to the rfpa's.

T4 has a dual purpose. Its primary responsibility is to act as an RF choke for both of the output transistors. Additionally, this transformer establishes a phase relationship between the drains of the two output transistors that is essential to the operation of transformer T3.

C19,C20,C22 and C26, C29, C30: These capacitors provide DC isolation between the drains of the output transistors and the load transformer.

C37, C39, L3, C38, C40. This network filters the +28V before it is presented to the drains of the output transistors. It also minimizes the amount of 1MHz fed back to the power supply (not to mention stage 1). Note that L3 is specially designed to handle the high currents (up to 5 amps) demanded by the output stage transistors.

T3: This part is the heart of the rfpa. It takes the outputs of the stage 2 transistors and combines them into a single sinusoid while also providing a 1:9 impedance transformation (transforming the 50 ohm load impedance into a ~5-6 ohm load for the output transistors). The transformer consists of tri-filar wire wrapped around a ferrite core.

C8,C2,L2,C1,C7: This is a maximally flat low pass filter with a cutoff of approximately 1.3MHz. Its purpose is to attenuate any 1MHz harmonics that may be present in the output. Even very low levels of 1MHz harmonic can significantly affect spectral peak widths (the rf loop detects harmonic energy and treats it as if it were 1MHz. Thus, the effective rf level at 1MHz is lower than it should be. Or conversely, the DC is too high. The result is

narrow peaks. Note that L2 is an air core coil. This was required because of the high power levels involved.

P2: The output BNC connection. The rfpa's output is routed to the coil box through this connector via 50 ohm coax.

P3 is the rfpa power connection. +28V, GND and sense lines are routed from the PDB to the rfpa through this connector.

NOTE: This page provides a running history of changes for a multi-page drawing which cannot conveniently be re-issued completely after each change. When making a change, list for each page all before and after numbers (within reason; use judgement, and use "extensive" revision note if loss of past history is tolerable, or retype complete page) and associate with each a symbol made up of the change letter and a serial subscript to appear here and on the page involved (there enclosed in a circle, triangle or other attention getting outline).

REV	QA	REVISIONS	APPROVED	DATE
A		AS RELEASED PER PCO23-6030	N. Moreyra	11/11/97

SPRITE SICB_LON Interface Theory of Operation

1.0 Overview

The purpose of this document is to provide some information on the hardware of the SICB-LON Interface Printed Circuit Assembly (G1946-60007).

The board has three main functions: bring Smartcard (05990-60410) communication to the bus board (G1946-60010) for distribution to the Detector (G1946-60011) and Analyzer (G1946-60001) boards, route power from the Power Distribution Board (G1946-60002) to Smartcard and the Bus Board, and to translate the SICB protocol from Smartcard to the LON protocol that is used for the Sprite Non-Real Time Subsytem bus.

2.0 Smartcard Communication

The SICB-LON interface board provides some simple logic to interface Smartcard to the rest of the system. Sprite uses the MSE bus feature of Smartcard. This is a parallel bus with 16 data lines and 8 address lines.

The logic itself is not, in itself, anything remarkable. What is important is the use of a latching octal transceiver (74ABT543) for the data lines. In the original design, the bus transceivers were not latching (74ABT245), the instrument data bus was not pulled high, and there were damping resistors in series with the data lines. This turned out to be the cause of a subtle problem which ended up causing a mass axis stability problem.

In the original design during a write to the Analyzer board (G1946-60001), when Smartcard released the instrument data lines (i.e. the data lines went into their tri-state mode), the Analyzer board bus transceiver output lines underwent a brief oscillation. When enough of the transceiver lines went into oscillation, the ground on the Analyzer board would be disturbed enough so that it would show up in the data. It was determined that the oscillation was due to the instrument data lines being tri-stated while the Analyzer board's transceivers were still enabled.

Once this problem had been identified, a latching transceiver was designed in, the damping resistors were removed, and the instrument data lines got pullup resistors. This eliminated the undefined state for the Analyzer board transceiver inputs and we no longer see the effect on the data.

Figure 1 shows a psuedo-timing diagram of the Read and Write signals for Sprite with the redesign. The top two traces are the Read and Write signals coming from Smartcard. The bottom two traces are the Read and Write signals that go to the Detector and Analyzer boards. The timing diagram is intended to only show the relationships between the control of the bus transceivers and the Read and Write signals.

The three middle traces are the control lines of the 74ABT543 bus transceivers. The G1, G2, and 1C5 inputs are grounded and are not shown on the diagram. The 2C6 trace is the latch enable signal for the Smartcard Write direction of the transceiver (Smartcard Write means Smartcard writing to the instrument). Note that this signal pulses low (pulse is ~50ns) during the Write cycle. This latches the Write information in the transceiver. The 2EN4 line is the output enable line of the transceiver for the Write direction. With this line low, the data is put out onto the instrument bus. Note that the only time this

goes high is during a READ operation and that the instrument bus is never in its tri-state mode during the WRITE operation.

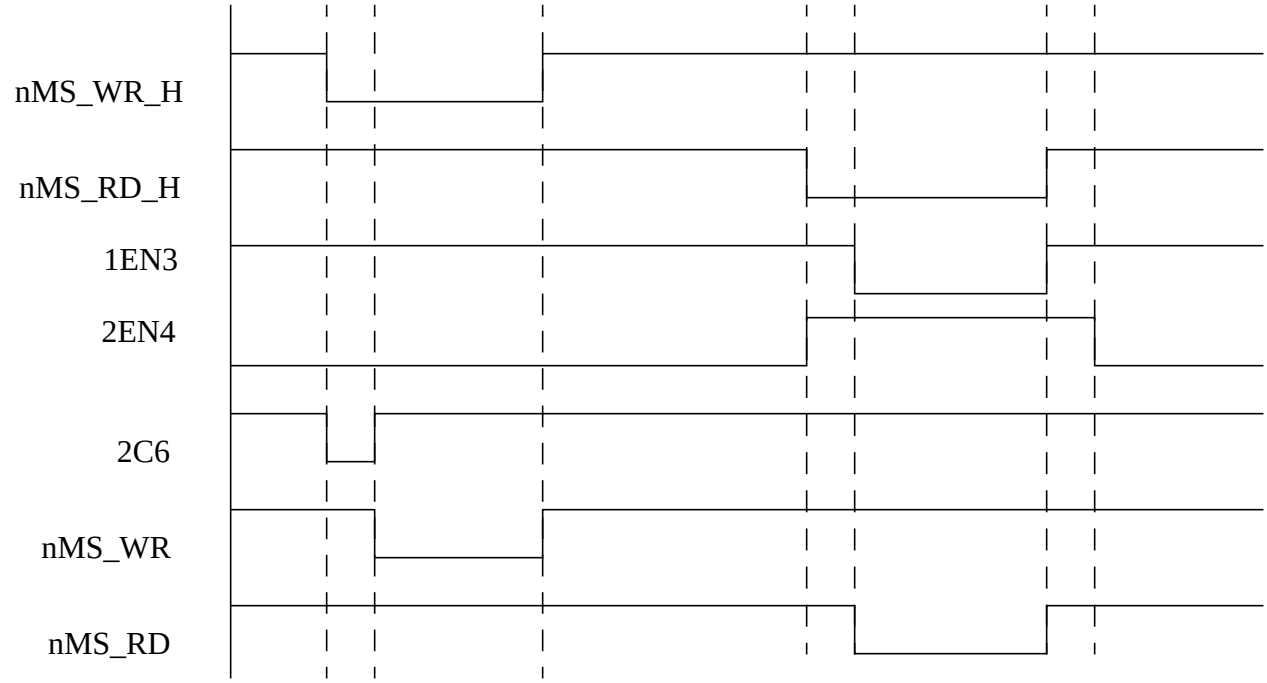

Figure 1: Psuedo Timing Diagram of Read and Write Signals

The data and address lines come through a 96 pin DIN connector (P1) and are listed in Table 1. Note that this is also where the Serial Instrument Command Bus (SICB) lines from Smartcard are delivered to the instrument. The lines come into pins 29A and 29B as denoted on the 60007 board. They come out of pins 4A and 4B on Smartcard. See the note at the end of Table 1 for an explanation of the pin numbering.

Table 1: G1946-60007 P1 pin assignments (to Smartcard II+)

Pin #	A	B	C
32	DCOM	DCOM	DCOM
31	DCOM	DCOM	DCOM
30	DCOM	1 MHz	1 MHz
29	LS_TxD*	LS_RxD*	nY_INT
28	DCOM	nTIMEOUT	nTIMEOUT

Table 1: G1946-60007 P1 pin assignments (to Smartcard II+)

Pin #	A	B	C
27	DCOM	nMS_WR_H	nMS_WR_H
26	DCOM	nPTF*	nPTF*
25	DCOM	nDCL*	nDCL*
24	MA[0]	nOFF_MS	nOFF_MS
23	DCOM	MS[15]	MS[15]
22	MA[1]	MS[14]	MS[14]
21	DCOM	MS[13]	MS[13]
20	MA[2]	MS[12]	MS[12]
19	DCOM	MS[11]	MS[11]
18	MA[3]	MS[10]	MS[10]
17	DCOM	MS[9]	MS[9]
16	MA[4]	MS[8]	MS[8]
15	DCOM	MS[7]	MS[7]
14	MA[5]	MS[6]	MS[6]
13	DCOM	MS[5]	MS[5]
12	MA[6]	MS[4]	MS[4]
11	DCOM	MS[3]	MS[3]
10	MA[7]	MS[2]	MS[2]
9	DCOM	MS[1]	MS[1]
8	DCOM	MS[0]	MS[0]
7	DCOM	nRESET*	nRESET*
6	DCOM	NC	NC
5	DCOM	nMS_RD_H	nMS_RD_H
4	VCC	VCC	VCC
3	VCC	VCC	VCC

Table 1: G1946-60007 P1 pin assignments (to Smartcard II+)

Pin #	A	B	C
2	DCOM	DCOM	DCOM
1	DCOM	DCOM	DCOM

Note: The G1946-60007 P1 connector is a DIN Type C connector (96 contact, Male, Right-Angle mount) that accepts Smartcard II+'s 96 contact, Female, Right-Angle mount connector. For some unknown reason, mating a right angle DIN to another right angle DIN requires that the pin numbers be reversed! If mating a right angle DIN to a vertically mounted DIN, the pin numbers match up correctly so there is no need for anything to be done in that case. Smartcard II+ has a right angle, Female DIN connector which necessitated reversing the numbers on P1 from the numbering on Smartcard.

* denotes an open collector driven line.

3.0 Power Distribution

The voltages to run Smartcard, the Detector board, and the Analyzer board comes from the Power Distribution Board (G1946-60002) through the SICB-LON Interface board. It is brought over to the Interface board via a flex circuit. Actually, the entire board is a rigid-flex circuit board with a flexible portion that plugs into the Power Distribution board. This was chosen to minimize the number of connections that the +5V supply would have to go through to reach Smartcard and the instrument boards (to minimize voltage drops).

The voltages come out of a custom power supply into which the Power Distribution Boards plugs in. The Power Distribution board puts these voltages on a 48 contact DIN connector (Female). The Interface board's flex circuit has the mating 48 pin DIN connector whose pin assignments are listed in Table 2. Pins 1C and 2C are not used. These pins were assigned when we brought the quadrupole heater through the Bus board (now an individual cable).

Table 2: G1946-60007 P3 Pin Assignments (to Power Distribution Board)

Pin #	A	B	C
1	DCOM	DCOM	HTR
2	DCOM	DCOM	HTR_RTN
3	DCOM	DCOM	DCOM
4	DCOM	HTR_SNS	SNS_RTN
5	DCOM	DCOM	DCOM

Table 2: G1946-60007 P3 Pin Assignments (to Power Distribution Board)

Pin #	A	B	C
6	VCC	VCC	VCC
7	VCC	VCC	VCC
8	VCC	VCC	VCC
9	ACOM	ACOM	ACOM
10	ACOM	-15V	-15V
11	ACOM	ACOM	+15V
12	ACOM	+15V	+15V
13	ACOM	ACOM	ACOM
14	DCOM	LONA	LONB
15	DCOM	+24V	+24V
16	nSHUTDN*	+24V	+24V

Note: P3 is a DIN Type C/2 connector (48 contact, Female, Right-Angle mount) that is mounted on the flexible portion of the 60007 Board and plugs into the Power Distribution Board. The Power Distribution Board has a vertically mounted DIN connector so the pin numbers match up correctly.

Once the power has come onto the Interface board, the majority of it is passed on to the Bus Board (G1946-60010) while some of the +5V is delivered to P1 for Smartcard. Power from the Power Distribution board and signals from Smartcard converge at the P2 connector. This connector plugs into the Bus Board where it is distributed to the Detector and Analyzer boards. Table 3 shows the pin assignments for this connector.

Table 3: Sprite J1 Pin Assignments (to Bus Board)

Pin #	A	B	C
1	NC1A	+24V	+24V
2	NC2A	+24V	+24V
3	ACOM	LONA	LONB
4	ACOM	ACOM	ACOM
5	+15V	+15V	+15V
6	+15V	+15V	+15V
7	-15V	-15V	-15V
8	ACOM	ACOM	ACOM
9	VCC	VCC	VCC
10	VCC	VCC	VCC
11	VCC	VCC	VCC
12	DCOM	DCOM	DCOM
13	DCOM	HTR_SNS	SNS_RTN
14	DCOM	DCOM	DCOM
15	HTR_RTN	HTR_RTN	HTR_RTN
16	HTR	HTR	HTR
17	DCOM	DCOM	DCOM
18	DCOM	NC18A	DG_CLK
19	DCOM	MA[1]	MA[0]
20	DCOM	MA[3]	MA[2]
21	DCOM	MA[5]	MA[4]
22	DCOM	MA[7]	MA[6]
23	DCOM	MS[15]	MS[14]
24	DCOM	MS[13]	MS[12]

Table 3: Sprite J1 Pin Assignments (to Bus Board)

Pin #	A	B	C
25	DCOM	MS[11]	MS[10]
26	DCOM	MS[9]	MS[8]
27	DCOM	MS[7]	MS[6]
28	DCOM	MS[5]	MS[4]
29	DCOM	MS[3]	MS[2]
30	DCOM	MS[1]	MS[0]
31	DCOM	nRESET*	nSHUTDN*
32	DCOM	nMS_RD	nMS_WR

Note: The Sprite J1 Connector is a DIN Type C connector (96 contact, Male, Right-Angle mount) which plugs into the Bus Board. All of the No-Connect lines should be individually tied to DCOM so that they don't float. The Bus Board has a vertically mounted DIN connector so the pin numbers match up correctly.

* denotes an open collector driven line.

4.0 SICB TO LON TRANSLATION

This is the last of the functions of the G1946-60007 board. A detailed look at the SICB protocol can be found in the MS Serial Instrument Command Bus ERS (A-G1946-90031-1). The SICB protocol is a byte passing protocol that does not care about the information that it is passing. It only cares about the number of bytes it passes.

This board recognizes SICB commands 9, 10, 11, and 12. Command 9 is sent to reset the Neuron chip on the Interface board. Command 10 is used to write data to the Interface board. Command 11 is not used. Command 12 is used to read data from the Interface board (a write is first performed and then data is read).

The format of the data that is written to the Interface board consists of a Command byte and, if any, data bytes. There are 66 commands that the Interface board understands. The specific commands are set forth in Table 4. More detailed comments pertaining to the individual nodes are contained in their documentation.

The Neuron chip uses its 11 I/O lines to communicate with the 8051 that implements the SICB protocol. Lines I/O0 - I/O7 of the Neuron chip are used to pass 8 bit data back and forth between the 8051 and the Neuron chip. The I/O10 line is used as the handshake line for read and write operations. In both the read and write cases, the Neuron is slave to the 8051.

An example of a write to the Neuron is shown in Figure 2. In this example, the 8051 initiates the operation by first putting the data on the I/O bus. The 8051 then indicates to the Neuron that data is available by bringing the Neuron's I/O8 line low. When the Neuron realizes its I/O8 line is low, it reads the data byte and acknowledges the transaction by setting its I/O10 line low. When the 8051 sees the acknowledge line go low, it sets the Neuron's I/O8 line high. When the Neuron sees its I/O8 go high, it sets its acknowledge line (I/O10) high and the handshake is completed.

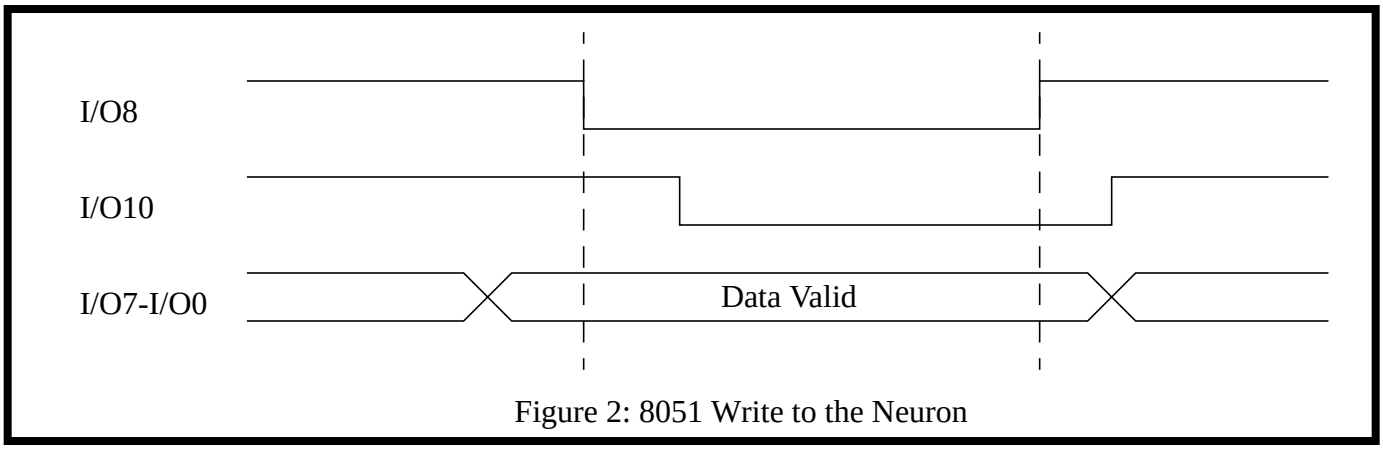

Figure 2: 8051 Write to the Neuron

An example of a read operation from the Neuron is shown in Figure 3. The 8051, again, initiates the transaction by bring the Neuron's I/O9 line low. When the Neuron detects its I/O9 line low, its data is put on the I/O bus and then it sets the acknowledge line (I/O10) low. When the 8051 sees the acknowledge line low, it read the data off of the bus and sets the Neuron's I/O9 line high. When the Neuron detects the I/O9 line high, it returns the acknowledge line to a high state and the handshake is completed..

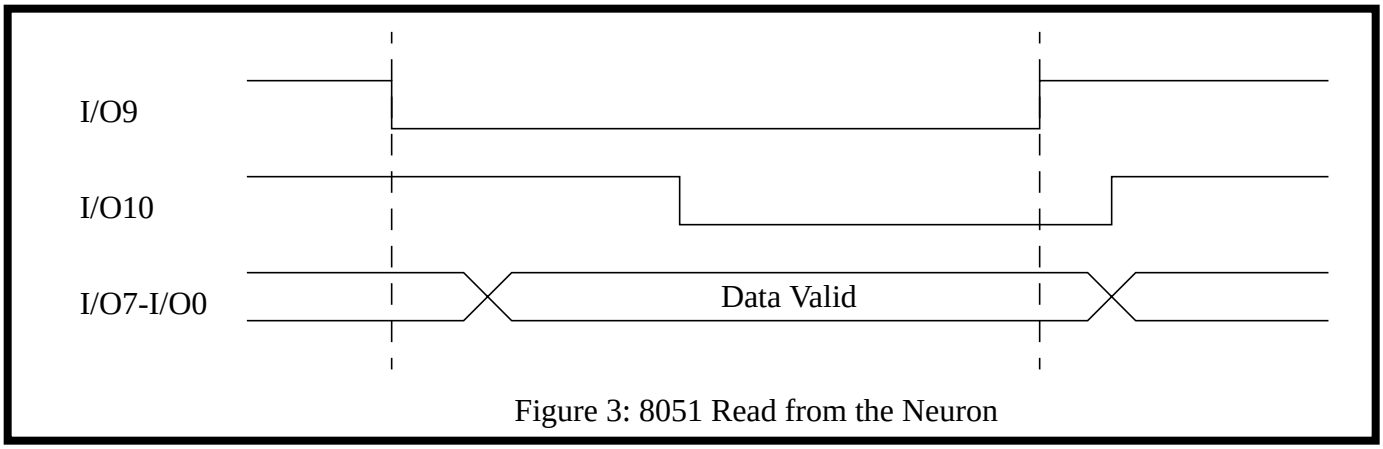

Figure 3: 8051 Read from the Neuron

All communication with the Neuron is a combination of the Read and Write Handshakes shown in Figures 2 and 3. As was mentioned earlier, the communication with the Neuron is always initiated by the 8051. The information that is passed back and forth is dependent on whether the 8051 is writing or reading data. It should be noted that since the 8051 always initiates a transaction, the first step of any transaction is a Write from the 8051 to the Neuron.

This is the Command Byte (not to be confused with the command byte in the SICB protocol). It tells the Neuron what is going to happen (read or write operation). If the 8051 is sending a temperature setpoint, for example, it would first write to the Neuron with a command number that would inform the Neuron that a temperature setpoint is coming. The Neuron would then know what to do with the information following the command byte and how many bytes to expect. If the 8051 wanted to read a pressure, the 8051 would first write a command to the Neuron which would inform the Neuron that a request was made for a pressure reading. The Neuron would then be ready to supply the data when the 8051 then issues a Read from the Neuron.

All the commands for the Neuron are predefined so the format of the data for the reads and writes are known by the host and Neuron. There is the assumption that the appropriate number of bytes are always sent or received and that the order is correct. After the Command byte, data is always sent or received with the most significant byte first. A list of all 66 commands is shown in Table 4. The complete LON interface specification can be found in the SICB-LON Interface ERS (A-G1946-60007-8).

Table 4: Host Commands for the LON System

Command	Neuron Operation To Host	# of Bytes, Data Format	Units	Description
1	Write	4 IEEE 754[1]	mbar	Report Pressure from Stage 1 Pirani Gauge
10	Write	5 ubyte[2], ulint[3], ulint		Report status of the Stage 1 Pirani Gauge[4] SO.on SO.warn SO.shutdown
11	Read	1 ubyte		Set operating mode for Stage 1 Pirani Gauge 0: Normal Mode Operation 1: Self Test Mode 2: Extended Test Mode Default: Diagnostic Mode
17	Read	ubyte		Event Select Number from Stage 1 Pirani Gauge Electronic Log Book

Table 4: Host Commands for the LON System

Command	Neuron Operation To Host	# of Bytes, Data Format	Units	Description
18	Write	12 ubyte, ulint, ulint, ulint, ubyte, ubyte, ubyte, ubyte, ubyte	 years, months, days, hours, minutes, seconds	<u>Report Event information for Stage 1 Pirani Gauge for event selected by command 17</u> SO.on SO.warn SO.shutdown, Time Stamp
19	Write	60 10 x ubyte, 10 x ubyte, 10 x ubyte, 10 x ubyte, 10 x ubyte, 10 x ubyte	 ASCII ASCII ASCII ASCII ASCII ASCII	<u>Report ID information for Stage 1 Pirani Gauge</u> Hardware Code # Software Code # Manufacturer Hardware Serial # OEM Part # Users tag
21	Write	4 IEEE 754	mbar	Report pressure from Stage 4 Ion Gauge
22	Read	1 ubyte		<u>Set ON/OFF state for Stage 4 Ion Gauge</u> 0: Turn off ion gauge 1: Turn on ion gauge (low emission) 2: Turn on ion gauge (high emission) 3: Degas ion gauge Default: Turn on ion gauge (low emission)
23	Read	4 IEEE 754	Pascal	Set foreline pressure interlock for Stage 4 Ion Gauge
30	Write	5 ubyte, ulint, ulint		<u>Report status information of Stage 4 Ion Gauge</u> SO.on SO.warn SO.shutdown

Table 4: Host Commands for the LON System

Command	Neuron Operation To Host	# of Bytes, Data Format	Units	Description
31	Read	1 ubyte		Set Operating Mode of Stage 4 Ion Gauge 0: Normal 1: Self Test 2: Extended Test Default: Diagnostic Mode
37	Read	ubyte		Event Select Number from Stage 4 Ion Gauge Electronic Log Book
38	Write	12 ubyte, ulint, ulint, ulint, ubyte, ubyte, ubyte, ubyte, ubyte	 years, months, days, hours, minutes seconds	Report Event information for Stage 4 Ion Gauge for event selected with command 37 SO.on SO.warn SO.shutdown Time Stamp
39	Write	60 10 x ubyte, 10 x ubyte, 10 x ubyte, 10 x ubyte, 10 x ubyte, 10 x ubyte	 ASCII ASCII ASCII ASCII ASCII ASCII	Report ID information for Stage 4 Ion Gauge Hardware Code # Software Code # Manufacturer Hardware Serial # OEM Part # Users tag
40	Write	5 ubyte, ulint, ulint		Report status information of LON Turbo I'face SO.on SO.warn. SO.shutdown
41	Read	1 ubyte		Set ON/OFF state for Turbo Pump Interface 0: Turn off turbo pumps Default: Turn on turbo pumps
42	Read	4 IEEE 754	Pascal	Set foreline pressure interlock for Turbo Pump Interface

Table 4: Host Commands for the LON System

Command	Neuron Operation To Host	# of Bytes, Data Format	Units	Description
43	Read	1 ubyte		Default: Any entry will cause Maintenance Timer 1 to reset to 0 but it is required that a byte be sent by the host for this command
44	Read	1 ubyte		Default: Any entry will cause Maintenance Timer 2 to reset to 0 but it is required that a byte be sent by the host for this command
45	Read	1 ubyte		Default: Any entry will cause the contents of the Maintence Output (MO) data structures to be copied into non-volatile memory.
46	Read	1 ubyte		Default: Any entry will initiate a poll of the MO1 and MO2 network variables. This is the only way to update the MO data copies in the SICB-LON Neuron.
47	Write	12 ubyte, ubyte, ubyte, ubyte, ubyte, ubyte,	 hours hours hours hours	Report the MO information for turbo 1 pump (in Sprite, this is the 250 l/s pump). Total time pump is on Total process time (not used) Total Time till service (not used) Process time till service (not used) Total number of ON/OFF cycles Total number of cycles till service (not used) This command should be preceded by command 46 to ensure the most recent information. Approximately 100ms should be allowed between commands 46 and 47. It would also be a good idea to issue command 45 to make sure this information gets put into non-volatile memory. Allow approximately 500ms before issuing another command after issuing command 45.

Table 4: Host Commands for the LON System

Command	Neuron Operation To Host	# of Bytes, Data Format	Units	Description
48	Write	12 ubyte, ubyte, ubyte, ubyte, ubyte, ubyte,	 hours hours hours hours	<u>Report the MO information for turbo 2 pump (in Sprite, this is the 70 l/s pump).</u> Total time pump is on Total process time (not used) Total Time till service (not used) Process time till service (not used) Total number of ON/OFF cycles Total number of cycles till service (not used) This command should be preceded by command 46 to ensure the most recent information. Approximately 100ms should be allowed between commands 46 and 48. It would also be a good idea to issue command 45 to make sure this information gets put into non-volatile memory. Allow approximately 500ms after issuing command 45 before issuing another command.
49	Write	60 10 x ubyte, 10 x ubyte, 10 x ubyte, 10 x ubyte, 10 x ubyte, 10 x ubyte	 ASCII ASCII ASCII ASCII ASCII ASCII	<u>Report ID information for LON Turbo Interface</u> Hardware Code # Software Code # Manufacturer Hardware Serial # OEM Part # Users tag
50	Read	1 ubyte		<u>Turn on Turbo Pumps</u> 0: Turn off both turbo pumps 1: Turn on turbo pump 2 2: Not used 3: Turn on turbo pump 1 4: Turn both turbo pumps on Default: Turn off both turbo pumps This command is only valid if the LON Turbo interface is in its Diagnostic Mode.

Table 4: Host Commands for the LON System

Command	Neuron Operation To Host	# of Bytes, Data Format	Units	Description
51	Read	1 ubyte		Set Operating Mode of LON Turbo Interface 1: Self test 2: Extended Test 3: Diagnostic Mode Default: Normal Mode
52	Write	2 ulint	Watts/10	Report Power consumption of Turbo 1 controller (data is reported in tenths of watts)
53	Write	2 ulint	Watts/10	Report Power consumption of Turbo 2 controller (data is reported in tenths of watts)
54	Write	1 ubyte	%/2	Report Speed of Turbo Pump 1 (data is reported in 0.5% resolution)
55	Write	1 ubyte	%/2	Report Speed of Turbo Pump 2 (data is reported in 0.5% resolution)
57	Read	ubyte		Event Select Number from LON Turbo Interface Electronic Log Book
58	Write	19 ulint, ubyte, ubyte, ulint, ulint, IEEE 754, ulint, ubyte, ubyte, ubyte, ubyte, ubyte	 %/2, %/2, watts/10, watts/10, mbar, years, months, days, hours, minutes, seconds	Report Event information for Lon Turbo I'face for event selected with command 57 Stop event word Turbo 1 speed (0.5% resolution) Turbo 2 speed (0.5% resolution) Turbo 1 power (tenths of watts) Turbo 2 power (tenths of watts) Stage 1 Pressure Time Stamp
61-65	Write	2 ulint		Commands 61-65 have been replaced by command 112. Zero is returned for these commands.

Table 4: Host Commands for the LON System

Command	Neuron Operation To Host	# of Bytes, Data Format	Units	Description
66	Write	7 ulint, ubyte, ubyte, ubyte, ubyte, ubyte	years, months, days, hours, minutes, seconds	Report Power Distribution Board's date/time stamp
68-72	Read	2 ulint		Commands 69-72 have been replaced by command 113. Nothing is done with the received data bytes.
73	Write	1 ubyte		Command 73 has been replaced by command 111. A zero is written in response to this command.
76	Read	1 ubyte		Set the Roughing Pump ON/OFF state 0: Turn off Roughing Pump Default: Turn on Roughing Pump
77	Read	1 ubyte		Report information from PDB on Main Power Supply (not used)
78	Read	7 ulint, ubyte, ubyte, ubyte, ubyte, ubyte	years, months, days, hours, minutes, seconds	Set Power Distribution Board's date/time stamp
79	Read	1 ubyte		Set calibrant delivery system mode
80	Read	1 ubyte		Set Stream Selection valve mode
87	Read	ubyte		Event Select Number from LON Turbo Interface Electronic Log Book

Table 4: Host Commands for the LON System

Command	Neuron Operation To Host	# of Bytes, Data Format	Units	Description
88	Write	15 ulint, ulint, ulint, ulint, ulint, ubyte ubyte, ubyte, ubyte, ubyte	 years, months, days, hours, minutes, seconds	<u>Report PDB event info (status, time/stamp data)</u> Status event word Warn even word Stop1 event word Stop2 event word Time Stamp
89	Write	60 10 x ubyte, 10 x ubyte, 10 x ubyte, 10 x ubyte, 10 x ubyte, 10 x ubyte	 ASCII ASCII ASCII ASCII ASCII ASCII	<u>Report ID information for PDB</u> Hardware Code # Software Code # Manufacturer Hardware Serial # OEM Part # Users tag
99	Write	60 10 x ubyte, 10 x ubyte, 10 x ubyte, 10 x ubyte, 10 x ubyte, 10 x ubyte	 ASCII ASCII ASCII ASCII ASCII ASCII	<u>Report ID information for SICB-LON Interface</u> Hardware Code # Software Code # Manufacturer Hardware Serial # OEM Part # Users tag
102	Read	16 array[0..15] of ubyte		16 byte diagnostic string which is sent to the PDB. Refer to PDB documentation for a description. Not needed for general operation
103	Write	16 array[0..15] of ubyte		16 byte diagnostic string which is read from the PDB. Refer to PDB documentation for a description. Not needed for general operation Note: msb of PDB response is set to 1 by command 102. Response is not valid until msb gets set to 0.

Table 4: Host Commands for the LON System

Command	Neuron Operation To Host	# of Bytes, Data Format	Units	Description
104	Write	32 10 x ubyte 6 x ubyte 8 x ubyte 8 x ubyte	 ASCII ASCII ASCII ASCII	Set Manufacturer ID info: Serial Number Quad Number Product Number Manufacture Date
105	Read	32 10 x ubyte 6 x ubyte 8 x ubyte 8 x ubyte	 ASCII ASCII ASCII ASCII	Report Manufacturer ID info: Serial Number Quad Number Product Number Manufacture Date
106	Read	1 ubyte		Set Autopumpdown ON/OFF 0: Turn Autopumpdown off Default: Turn Autopumpdown on
108	Write	4 IEEE 754	mbar	Report pressure from Stage 2 Pirani Gauge (Only used during Manufacturing test)
109	Write	4 IEEE 754	mbar	Report pressure from Stage 3 Ion Gauge (Only used during Manufacturing test)
110	Read	1 ubyte		Set ON/OFF state for Stage 3 Ion Gauge 0: Turn off ion gauge 1: Turn on ion gauge (low emission) 2: Turn on ion gauge (high emission) 3: Degas ion gauge Default: Turn on ion gauge (low emission)

Table 4: Host Commands for the LON System

Command	Neuron Operation To Host	# of Bytes, Data Format	Units	Description
111	Write	23 ubyte, ulint, ulint, ubyte, ulint, ulint, ubyte, ulint, ulint, ulint, ulint, ulint, ulint		Report All Status Stage 1 Pirani Gauge: *SO.on* *SO.warn* *SO.shutdown* Stage 4 Ion Gauge: *SO.on* *SO.warn* *SO.shutdown* Turbo Interface: *SO.on* *SO.warn* *SO.shutdown* PDB: *SO.status* *SO.warn* *SO.shut1* *SO.shut2*

Table 4: Host Commands for the LON System

Command	Neuron Operation To Host	# of Bytes, Data Format	Units	Description
112	Write	46		Report all sensor outputs
		IEEE 754	mbar	Stage 1 pressure
		IEEE 754	mbar	Stage 4 pressure
		ubyte,	%/2	Turbo pump 1 speed (to 0.5% Full Scale)
		ubyte,	%/2	Turbo pump 2 speed (to 0.5% Full Scale)
		ulint,	watts/10	Turbo pump 1 power (tenths of watts)
		ulint,	watts/10	Turbo pump 2 power (tenths of watts)
		array[0..31]	deg C	0,1: Quad Temp Reading (MSB first)
		of ubyte	deg C	2,3: Drying Gas Temp Reading (MSB first)
			deg C	4,5: Vaporizer Temp Reading (MSB first)
			psi/10	6,7: Drying Gas Pressure Reading (MSB first)
			psi/10	8.9: Nebulizer Gas Pressure Reading (MSB first)
			%/65535	10,11: Quad Temp duty cycle
			%/65535	12,13: Drying Gas Temp duty cycle
			%/65535	14,15: Vaporizer Temp duty cycle
			%/65535	16,17: Drying Gas Pressure duty cycle
			%/65535	18,19: Nebulizer Gas Pressure duty cycle
			rpm	20: Electronics Fan Speed
			rpm	21: Turbo Fan Speed
			rpm	22: Power Supply Fan Speed
			volts	23: 110VAC Level
			deg C	24: RFPA Heat Sink Temperature (not used)
			hertz	25: Power Line Frequency
				26-30: Spare
113	Read	16		Set all zones
		array[0..15]	deg C	0,1: Quad Temp Setpoint
		of ubyte	deg C	2,3: Drying Gas Temp Setpoint
			deg C	4,5: Vaporizer Temp Setpoint
			psi/10	6,7: Drying Gas Pressure Setpoint (tenths of psi)
			psi/10	8,9: Nebulizer Gas Pressure Setpt (tenths of psi)
				10-15: Spare

Table 4: Host Commands for the LON System

Command	Neuron Operation To Host	# of Bytes, Data Format	Units	Description
114	Read	10		Set Control Parameters for Turbo Interface
		ulint,	watts/10	Zero Threshold for Power Reporting
		ulint,	seconds	Time allowed to reach 50% speed before error
		ubyte,	seconds	Time to wait before checking if speed decreased
		ubyte,	seconds	Time to wait before checking speed
		ubyte,	%/2	Full On Threshold for Pumps 1 and 2
		ubyte,	%/2	Hysterisis after pump speed passes Full On
		ubyte,	%/2	Hysterisis after pump speed passes 50%
		ubyte	%/2	Speed Threshold for zero speed
115	Write	10		Set Control Parameters for Turbo Interface
		ulint,	watts/10	Zero Threshold for Power Reporting
		ulint,	seconds	Time allowed to reach 50% speed before error
		ubyte,	seconds	Time to wait before checking if speed decreased
		ubyte,	seconds	Time to wait before checking speed
		ubyte,	%/2	Full On Threshold for Pumps 1 and 2
		ubyte,	%/2	Hysterisis after pump speed passes Full On
		ubyte,	%/2	Hysterisis after pump speed passes 50%
		ubyte	%/2	Speed Threshold for zero speed

1. IEEE 754 format consists of 1 sign bit, 8 exponent bits, and 23 mantissa bits (total of 4 bytes)
2. ubyte is an unsigned byte (valid range from 0 to 255)
3. ulint is an unsigned long integer (valid range from 0 to 65535)
4. Structures are defined in detail in the documentation for the individual nodes

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REV	REVISIONS	APPROVED	DATE
A	AS ISSUED PER PC23-6030	N. Moreyra	08/01/97

R. Roushall DRAWN BY	07/29/97	**Octopole Driver Assembly Theory of Operation** TITLE	HEWLETT PACKARD
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N. Moreyra RELEASE TO PROD.	08/01/97		G1946-60009 PART NUMBER
SUPERSEDES DWG.	CURRENT REV A	PAGE 1 OF 8	**A-G1946-60009-5**

THEORY OF OPERATION
A-G1946-60009-5

Introduction:

The assembly, G1946-60009, is referred to as the octopole driver for the SPRITE instrument. The main function of this assembly is to drive a RF and DC voltage to the octopole assembly in the source of SPRITE. Through various investigations of the chemists on SPRITE, it was determined that the octopole assembly would need a varying RF voltage of 0 to 300 volts peak-to-peak at ~2.5 Mhz and a varying +/- 20 volts DC of common voltage. The RF voltage is applied in such a way as to provide one phase on one set of rods, and a 180^{o} phase on the other set of rods. The DC voltage is a common voltage to offset the entire assembly.

The rods are organized in a circular fashion with eight rods parallel to each other. Every other rod is connected together such that one set of rods carry one AC/DC voltage pair, and the other set of rods carry the other AC/DC voltage pair. The following diagram shows the orientation of the rods and their connections.

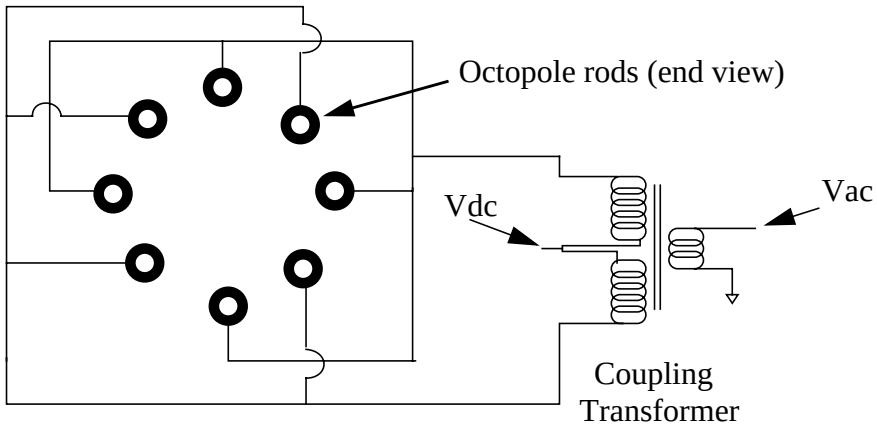

Figure 1. Octopole Connection

As shown in Figure 1, one method to achieve the AC/DC pairs is to use a transformer to couple in the Vac and Vdc signals. This will provide the 180^{o} phase shift as well as float a DC voltage common on all rods.

Schematic Sheet:

There is only one schematic for this assembly. The schematic shows all of the voltage generation and control to derive the Vac and Vdc signals. There are essentially six (6) sections of the schematic that outline all

of the functionality of the assembly; 1) Power, 2) RF Drive, 3) RF Detection, 4) Error Amp and Shutdown, 5) Knee Control, and 6) Fault Detection. The best way to read the following descriptions is to have the schematics in hand.

Power

There are four power signals and two grounds sent to this assembly. The powers are +5v, +15v, -15v, and +24v. The grounds are DCOM and ACOM. The power signals +5v and +24v are associated with DCOM and the power signals +15v and -15v are associated with ACOM. The +5v signal is only used on the Shutdown circuit, however, it is brought out to this board as a testpoint since this board provides the power testpoints for probing a SPRITE instrument. The +24v power signal is first series filtered by a ferrite, E2, to minimize RF current noise, and then filtered by capacitors C7, C20, C21, and C22 to minimize voltage noise. The +24v provides power to the RF power amplifier and a bias voltage to the fault detection circuits. The +15v and -15v power signals are used to power the opamps on the assembly. The ACOM and DCOM signals are joined by a diode, CR7. This allows for the grounds to operate separately, but keeps them from getting more than a diode drop apart.

RF Drive

The RF Drive circuit consists of the components needed to generate and drive a ~2.5 Mhz, 0 to 300v peak-to-peak signal to the octopole. The first section of the drive circuit is the oscillator. Y1 is a 2.4576 Mhz quart oscillator which together with Q2, R4, C2, and C3, make up a colpits oscillator. The signal out of Q2 pin 3, is AC coupled to the second section, a biased, buffer amplifier stage made up of Q3, R5, R15, C14, R6, and R7. This stage increases the power of the AC signal to drive the power amplifier stage. The signal out of Q3 is first filtered by L1 and C15 to create a sinusoidal ~2.5 Mhz signal. This signal then drives the third stage, a power transistor Q4. Q4 is designed as a high gain class A amplifier to amplify the ~2.5 Mhz signal. The emitter leg has low DC impedance setup by R8 and R9. C34 is used to increase the AC gain of the transistor. L3, pulled on by Q4, is used as a choke on the 24v supply and as the voltage multiplier. The back EMF from L3 acts to nearly double the +24V to +48V when Q4 releases. This drive point is then AC coupled to the load of the coupling transformer, T1. The transformer is a 2-to-18 step up transformer used to generate the 300 volts needed on the octopole.

The transformer is the major element that makes this circuit work. As shown in figure 1, the transformer is connected directly to the octopole assembly. The octopole is modeled as a capacitance between the rods and two capacitances to ground. The transformer is modeled as an inductor in parallel with the capacitance of the octopole assembly. Since the capacitance of the octopole is fixed by the mechanical design and the leads, the inductor is chosen to resonate at ~2.5 Mhz. More turns on the secondary windings of the transformer will increase the inductance. The optimum number of turns was determined to be 18. To adjust for any variances, a gapped POT core was chosen. By turning the adjustment screw, the inductance will change to fine tune the resonant point. It is very important that the pot core is adjusted to make the resonance at ~2.5 Mhz. At resonance, the load of the transformer on the amplifier becomes real (no phase) and maximum (largest impedance). With a large, real load, the power amplifier is able to drive large voltages with minimal power. The adjustment procedure will be described later in this document.

RF Detection

Since the RF Drive amplitude is very important in the octopole design, the RF amplitude is sampled and feed into a closed loop feedback control system by the RF Detection components C30, C31, CR5, and CR6. The capacitors provide a RF sample of current of both phases of the RF signal. The larger the RF voltage, the more current is sampled through C30 and C31. The diodes CR5 and CR6 rectify the two phases of the signal. C32, L4, C29, and R50 provide a filter to create an average DC current signal that is proportional to the peak-to-peak voltage of the RF signal. To determine the average current that relates to the peak voltage, the following relationship must be solved:

$$Iav = \frac{1}{T}\int_0^T i\,dt$$

This equation is the definition of the Average current of a periodic signal. Since the voltage we are sampling is a sinusoidal signal and rectified, we can simplify the equation to the following:

$$Iav = \frac{1}{\frac{1}{2}T}\int_{-\frac{T}{4}}^{\frac{T}{4}} I_{max}\cos\frac{2\pi t}{T}\,dt$$

This integral gets evaluated to:

$$Iav = \frac{2}{\pi}I_{max}$$

We can further manipulate this relationship to include the peak voltage of the RF signal.

$$Iav = \frac{2}{\pi}(V_{max}\omega C)$$

In this design, C is 3.3 pf, and the frequency is 2.4576 Mhz. The above equation relates the peak voltage to the average current out of the detect signal. Since the peak voltage is one-half the peak to peak voltage, the final relationship is:

$$Iav = 2V_{pp}fC$$

We now have a relationship for average current (*Iav*) out of the detect circuit versus peak-to-peak voltage (*Vpp*) on the octopole. The following table gives some typical values of current and voltage. The maximum peak-to-peak voltage allowed in this design is 300V.

Table 1: Typical Voltage/Current of Detect Circuit

Vrfpeak	Iav	Vpp	Imax
-977mV	1.62mA	100V	2.55mA
-2.93V	4.87mA	300V	7.64mA
-5.0V	8.30mA	512V	13.05mA

Error Amp and Shutdown

The average current out of the detect circuit is fed into the virtual ground of the opamp U2. This amp is configured as an integration amplifier setup by components C33 and C38. CR2 is used to keep the opamp in control should the detect current become larger than the control current. The control current is established by resistors R52 and R53. The resistance value was chosen such that a -5v control voltage would create a 512pp voltage on the octopole. Since the DAC driving the control voltage is 12 bit, 1 LSB is 125 mV pp. The voltage out of the Error Amp drives Q5 which applies a bias voltage to the colpits and buffer stage amplifiers of the RF Drive circuit. This increase in voltage will increase the peak-to-peak voltage on the octopole.

Q1 and CR4 form a fast shutdown circuit for the octopole RF. When the OCT_OFF signal is asserted, Q1 will turn on and short out the gain of the Error Amp such that it will not put out any drive voltage.

Knee Control

The knee circuit is a electronic method of varying the RF peak-to-peak voltage on the octopole. The purpose this circuit is to lower the RF voltage linearly with respect to lower mass. It performs this function by summing into the error amp a current that is opposite the control current. Opamp, U2, drives a 0 to 10v signal across the summing resistor, R41, to offset the control current. Since the control circuit is 0 to -5v and the opamp is 0 to +10v, R41 is twice the value of the parallel combination of R52 and R53.

The knee circuit is controlled by two signals, O_KNEE and MASS_SETPT. O_KNEE is generated by a 12 bit DAC with a range of 0 to -5v. This signal is in units of MASS to correspond to a mass position where the knee occurs. MASS_SETPT is a 0 to 10v signal that relates to the mass position. 0v is 0 AMU and 10v is 3275.75 AMU. This signal is derived from the main 16 bit mass DAC. Figure 2 gives an example of the peak-to-peak voltage versus mass when the Knee and Peak Control functions are applied. The RF peak voltage is set by the control signal RFPEAK, and the Knee is set by the control voltage O_KNEE.

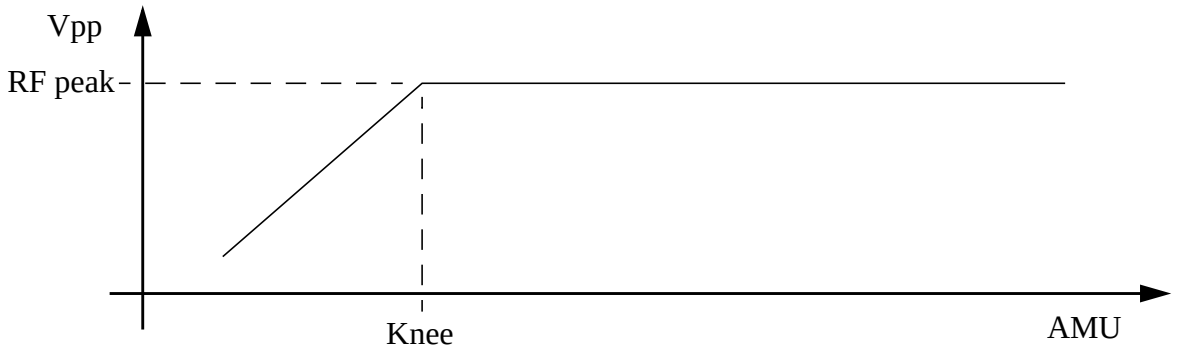

Figure 2. Octopole Driver Operation

When the mass is above the knee setting, the RF voltage on the octopole is determined by the RF peak voltage. When the mass setting is below the knee setting, the RF voltage on the octopole is less than the RF peak voltage. The slope at which the voltage falls off is ~1.1 volts per AMU. The opamp, U2, together with R46, R45, R44, R54, R37, and CR1 accomplishes the task. The following discussion will explain how the knee function is generated.

To start off with, the knee circuit can be simplified to make the analysis easier. Figure 3 is a simplified version of the circuit.

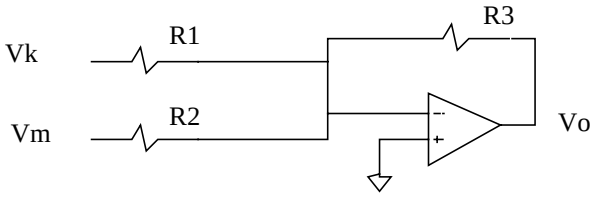

Figure 3. Simplified Knee Circuit

In Figure 3, Vo is the output voltage (0 to +10v), Vk is the knee voltage (0 to -5v), and Vm is the voltage relating to mass position (0 to +10v). The equation that relates Vo to Vk and Vm is:

$$Vo = -\frac{R3}{R1}Vk - \frac{R3}{R2}Vm$$

To solve this equation for the unknown resistor values, a few given relationships are needed.

1) Slope of pre-knee is 1.1 volts per amu.
2) When Vm = 0 and Vk = 465.45 AMU, then Vo = 10v (Vrf is 0 volts for a 512 volt setting).
3) When Vm = 465.45 AMU and Vk = 465.45 AMU, then V0 = 0v.

With these conditions, substitute item 3) into the equation to come up with the following:

$$Vo = -\left(\frac{R3}{R1}\frac{(465.45 \cdot -5)}{4096}\right) - \left(\frac{R3}{R2}\frac{(465.45 \cdot 10)}{3276.75}\right) = 0$$

This equation simplifies to:

$$R2 = 2.5 \cdot R1$$

Using relationship 2) above:

$$\frac{(R3)}{R1}\frac{(465.45 \cdot 5)}{4096} - 0 = 10$$

Solving for R3 gives the following:

$$R3 = 17.6 \cdot R1$$

Using the resistor values out of the LMC preferred parts manual, resistances were chosen for R45, R46, and R44 on the schematic. R3 from the simplified model is the parallel combination of R54 and R37 of the schematic. The diode, CR1, keeps the knee circuit from "adding" to the control signal, RFPEAK, and it keeps the opamp in the positive voltage domain.

Fault Detection

The fault detection circuit consists of U1, R43, R51, R11, R24, and CR3. A fault is generated if the Error Amp drives much above 11 volts. This implies that the RF peak-to-peak voltage can not be reached due to a problem on the board or in the octopole assembly. When this occurs, the voltage on the minus side of U1 exceeds the voltage on the positive side and the open-collector output will go low to trigger a fault on the analyzer board, G1946-60001. Resistors R43 and R51 bias the positive side of U1. CR3 is used to keep the minus side of U1 from going below the rail voltage.

Testpoints:

This board is mounted near the top of the SPRITE electronic tub. Because of this, testpoints were placed on this board to monitor power and ground. Also, a testpoint is provided for the mass axis voltage as a means to probe the operation of the instrument. There are also testpoints for monitoring the drive level out of the error

amp and the knee voltage. The drive level is very important in tuning the coupling transformer to the octopole.

As mentioned in the RF DRIVE section, the transformer is a gapped transformer with an adjustment slug. The proper way to adjust the transformer is as follows:

1) Make sure the assembly is properly connected to the instrument.

2) Put a volt meter across the DRIVE and ACOM testpoints. This will measure 0 to +10 volts.

3) Set the Octopole Knee value to 0 AMU.

4) Set the mass position to 50 AMU or greater. This really doesn't matter since the Knee is 0.

5) Set the Octopole peak value to 50 volts.

6) Adjust the transformer slug to minimize the voltage reading.

7) Repeat item 6) at higher voltage settings.

The design of the octopole driver can drive to 300 volts peak-to-peak with some margin in the Error Amp. However, the design does not have enough drive to get much above 350 volts. To get more voltage drive, the primary of the transformer could be reduced to one turn. This will make the drive transistor drive harder, so caution should be considered before trying this. Typically, the DRIVE point will read below 9 volts when the peak to peak voltage is set to 300 volts. When the DRIVE point reaches 10 volts and above, the fault circuitry is close to tripping.

Miscellaneous:

There are a few items on the board that provides options for controlling the octopole. First of all, there are two jumpers on the board, P15 and P16. These jumpers provides options for controlling the output transformer. There are two DC drive signals to split the secondaries of the transformer. For SPRITE, the DC drives are shorted together to make a common DC offset on the octopole. This is accomplished by a jumper on P15. There are also some filter capacitors, C38 and C39, to filter any RF signals off the DC drive lines. For SPRITE, these filters are not needed, therefore, no jumper is placed on P16.

The second miscellaneous function is the balance on the RF Output voltage of the transformer. Capacitors C27 and C28 act as load capacitors to help balance the octopole. The mechanical design of the octopole has more capacitance on one side of the rods than the other. Because of this, one of the load capacitors (C28) is loaded to help balance the load. Should the octopole mechanical design change, these load capacitors should be reevaluated.

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SUPERSEDES DWG.	CURRENT REV A	PAGE 1 OF 5	**A-G1946-60009-6**

Engineering Report
G1946-60009-6

This document will describe details not discussed in the Theory of Operations document. There will be some notes on design decisions and reasons for designing this card.

This design is called the octopole driver assembly. Its main purpose is to provide a AC and DC voltage to a set of rods in the source of SPRITE. The rods act as an ion guide and help focus ions into the Quad. At the time of the design, it was more cost effective to design our own driver than to buy some sort of RF Power Amplifier. In designing our own, we were able to add features such as the Octopole Knee feature. We were also able to provide testpoints for easy access of probing the power supply signals. The Theory of Operation outlines the functionality of the card and describes most of the design ideas. However, this report will describe the theory behind the design as well as point out some thoughts about future revisions of this design. The main areas of focus will be on the features and the RF transformer.

Design Theory:

To transmit ions, the octopole must be driven with a RF voltage. As discussed in the theory of operation, the RF voltage must vary with mass. The variance in RF voltage was accomplished with a KNEE circuit that gave a slope of 1.1 volts per AMU. The 1.1 volt per AMU slope was predetermined from experiments performed on LP units of SPRITE. The reason that the voltage needs to be lower for smaller masses has to do with the maximum transmission of ions versus RF voltage for the different masses. For larger masses (above 300 amu typically), the maxima versus voltage is very broad in that >90% of the ions are transmitter through the octopole for a RF voltage range of 200 to 300+ volts. For smaller masses, particularly below 150 amu, the maxima versus voltage is very small and is of low RF voltage. For example, a 69 amu ion may only transmit for a voltage of 40 volts RF with only 5 to 10 volts of range. Figure 1 resembles a rough estimate of what the transmission curves look like.

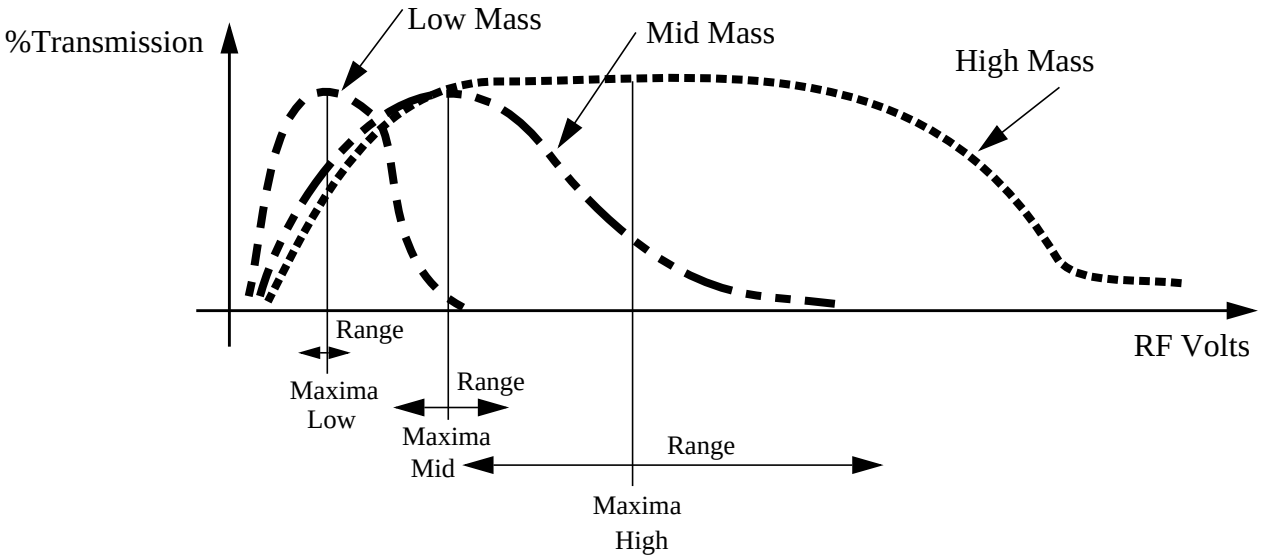

Figure 1. Octopole Transmission Curves

Kent Henry determined from his experiments, that an approximation of a slope of 1.1v per AMU below the knee setting and a fixed voltage above the knee setting would roughly maximize the transmission of ions through the mass range as shown on figure 2.

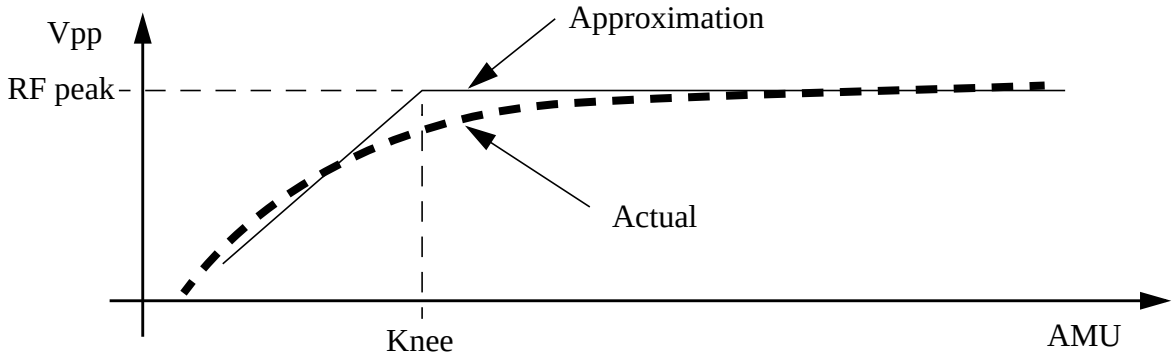

Figure 2. Transmission Curve

Features:

There are two main areas where features were added to improve functionality; 1) Knee Circuit, and 2) the common DC drive.

The Knee circuit was added to create an approximation of the transmission curve needed to maximize transmission of all masses. There are several reasons why we should have not done it this way. First of all, the approximation of the curve was determined from LP and early PP instruments. The mechanical aspects of these

instruments are slightly different than the released versions of the instrument. Also, the curve was experimentally determined to be 1.1 volts per AMU by "averaging" the results of a few instruments. These results did point out that not every instrument exhibits the same response. Another reason to not implement the knee function this way is that the analog design is not perfectly determined. The resistors have a 1% tolerance which can throw off the slope of the line very slightly. As pointed out in the Theory of Operation, the relationships of the resistors need to be very precise to get exactly 1.1 volt per AMU. The resistors chosen do not exactly fit the relationships. All of these approximations caused problems in early production units. First of all, the chemist involved in the design provided an algorithm on how to calibrate the peak and knee settings. The algorithm did not account for variations and tolerances from system to system. Lastly, the transmission curve is a exponential curve and not a linearized curve. Figure 2 shows the plots of the approximation versus the actual curve. As you can see from the graph, the approximation doesn't fit the relationship too accurately.

Given the circuit that exists, the best way to calibrate the octopole parameters is as follows:

1) Generate low mass ion(s), either a tune compound or a fragment ion.
2) Set the octopole knee parameter to 290 AMU.
3) ramp the octopole peak voltage on the low mass ion(s).
4) Pick the appropriate octopole peak voltage from the ramp. DONE.

This procedure will allow the maximum transmission of low mass ions, which are most critical, and still allow very good high mass transmission. By ramping the octopole peak voltage, all of the tolerances and variations in the mechanical and electrical design are removed.

There is also a better way to create the transmission curve. Since we have the ability to ramp a lens element, the octopole peak voltage could just be ramped to give the exact transmission curve needed for the instrument. By creating a dynamic ramp of octopole peak voltage, the knee circuit is not needed at all. This should be considered on the next revision of the board.

The common DC drive is the other feature that was added for flexibility. The jumper, P15, is currently shorted together to common both phases of the coupling transformer. If the jumper is removed, then separate DC voltages can drive the two phases. This could be used to make the octopole be a high pass filter or even a low resolution ion filter. The current design does not lend itself very well for this flexibility. The jumper will physically short the two DC drive signals which is not good! A better way to do this would be to build a three-pin jumper that would common the transformer on one DC drive signal. That way, when the jumper is applied, the two phases will be connected to only one DC drive signal as shown in figure 3.

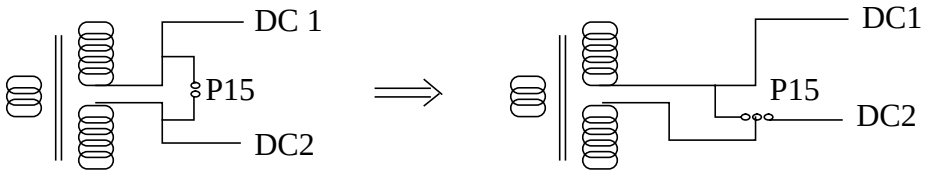

Figure 3. DC coupling of transformer

This method is used on the Esquire-LC design to couple in two DC voltages. This is a much better method and it should be considered on the next revision of the board.

RF Transformer:

One of the key elements of the whole design is the RF Transformer. This design is based on the fact that the secondaries of the transformer are resonant with the capacitance of the octopole. During the course of the project the octopole assembly changed many times which required the turns ratio to change. Also, the type of core material, wire, and the method of winding all have an effect on the inductance of the transformer. These parameters are important and should be chosen carefully. For example, if the two secondaries are wound separately, then the parasitic capacitance in minimized, but the voltage matching is not very tight. If the secondaries are bifilar wound, then the voltage matching is very tight, but the parasitic capacitance increases and the voltage isolation decreases.

There are also other ways to mount the transformer than the method chosen. The current method uses a metal mounting bracket to hold the transformer on the board. However, the leads are loose and need to be hand soldered. There are mounting brackets available that convert the part to a leaded through-hole part for board mount. This would make it easier for manufacturing to have a through-hole assembly to load as opposed to a hand loaded part.

The last concern with the transformer has to do with the adjustment screw. This screw is used to dip the inductance to minimize the drive voltage required for a given voltage. If the screw is driven all the way into the part, it actually hits the blank board before it has utilized the full adjustment range. The next spin of the board should make a drill hole in the middle of the transformer to allow the screw threads to go through the bottom of the board without falling out the end.

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Overview: This document describes the theory of operation behind the G1946-60011 detector PCA.
The G1946-60011 detector PCA provides the following functionality:

1) HED supply control. The detector PCA has a 20 pin ribbon cable connection for the HED supply. +24V, enable, control voltage, and a fault readbacks are all routed to the HED supply through this connector. The enables and fault handling are controlled by a Xilinx 7336 programmable logic part that resides on the detector PCA (G1946-80055).

2) CDEM supply and control circuitry. The gamma CDEM (detector high voltage) supply is mounted on the detector board.

3) Log amp interconnect and control. Chip selects and various other signals for the log amp are generated by the Xilinx 7336. A socket connector mounted on the back side of the detector PCA provides a mounting point for the log amp.

4) Logic Analyzer pod connection. 2 connectors on the detector PCA provide interconnect for the logic analyzer. Note that the connectors are mis-labeled. The pod for address lines should be connected to the connector labeled "DATA" and the pod for data lines should be connected to the connector labeled "ADDRESS."

This board is rather simple; this discussion will therefore be brief. The remainder of this document discusses the board schematics. The above functionality is outlined by addressing each component on the board in detail.

Sheet1: Sheet 1 contains the log amp connector, logic analyzer pod connections, HED connector, a dual DAC, and the CDEM module.

U4: This part is a simple zener voltage reference. It provides a -10V reference for the dual DAC. R5 provides a minimum current path to keep the zener in break down.

U6. This part is a dual 12 bit DAC. Internal registers latch values written to either DAC. The data pins of the DAC sit on the MSE bus; chip selects are generated by the Xilinx 7336. U4 generates an external -10V reference. Using a negative reference simplifies the analog output circuitry (U5). The analog outputs of this DAC are used to control the output levels of the HED and CDEM supplies.

U5. This AD706 dual precision op amp is used to convert the current output of DAC U6 to voltage output. The output voltages are then used to drive the HED and CDEM supplies.

P3. This jumper is used with obsolete prototype high voltage supplies to enable/disable ramping. It is not used at this time.

CR1, R1, R2: These 3 components are used to protect the output pins of the Xilinx 7336 from excessive volt-

ages that may be present on HED output enable pins (the HED supply has an internal 3kohm resistor pulling this line up to 9V).

P4: This 20 pin ribbon cable connector provides a connection for the HED 10kV supply. Power, level control, enable, polarity control, and fault signals are routed through this connector.

P6: This jumper was used with gamma HED supplies. These supplies are no longer supported.

J1: This jumper allows the board to be configured for fixed HED (10kV, no jumper) or rampable HED (DAC output voltage routed to HED control input--jumper should be inserted over pins 1 and 2). Note that the silk screen information on the actual PCA is incorrect and should be ignored. This text will be changed on the next roll of the board; it was not deemed necessary to roll the board simply for the silk screen.

P5: This connector is for the log amp PCA. The log amp PCA is mounted to the detector PCA through this connector. The MSE data bus, lower address bus nibble, various chip selects and enables, and log amp power are routed through this connector.

P1: P1 provides a logic analyzer pod connection for the data lines of the MSE bus.

P2: This connector provides a logic analyzer pod connection for the address lines of the MSE bus.

CR2, R3, R4: These 3 components are used to protect the Xilinx 7336 from excessive voltages that may be present on the CDEM output enable line.

U1: This is the CDEM high voltage supply. This supply provides up to 3kV of voltage for use with the mass specs electron multiplier. The output voltage of this part is controlled by the CNTL_CDEM analog voltage. This voltage is generated by DAC U6. Connector P7 is used to route the 3kV to the detector feedthrough on the vacuum manifold.

Sheet 2: Sheet 2 contains the mother board connection (through which all power and signals are routed to the board), and all of the logic that provides detector board functionality.

J2: This connector is a 96 pin connector. It mounts on the bottom of the detector board and allows it to plug into the mother board. Power for the board and MSE bus signals are routed through this connector. Table 1 provides a brief description of signals pertinent to the detector PCA.

U11/U10. These parts are 555 timers wired in a one shot configuration. Previous versions of the detector board used these one shots to hold off CDEM and HED faults whenever the DAC voltages were changed. The one shots were triggered whenever the HED or CDEM DAC's were written to. Faults for these supplies were then ignored during the one shot interval (these supplies will trigger faults when their output voltage is moving). This function is currently performed by a counter circuit within the Xilinx 7336. Thus these parts have no real function at this time other than to blink the HED and CDEM one shot LED's (this gives a visual indication of writes to either the HED or CDEM).

U9 is a dual flip flop. It is used to latch the CDEM and HED mask bits. Discrete flip flops were used to reduce the node demand within the 7336 (i.e. there wasn't enough room inside the programmable part). The trigger for the flip flops are generated by the 7336 whenever MSE writes at address 6 occur. Both flip flops are reset in the event of activity on the nRESET_MB line.

Q1: This NPN transistor is used to pull the system shutdown line low. The 7336 will drive this transistor whenever valid CDEM or HED faults occur.

U8: This is the 7336 Xilinx programmable part (G1946-80055). This programmable part contains most of the detector PCA's logic. It is responsible for MSE address decoding and fault handling. See the G1946-80055 theory of operation for a detailed discussion of this part.

Table 1:

Signal	Purpose
+24V -15V +15V VCC(5V) ACOM DCOM	These lines provide power for the detector PCA. +24V and VCC are referenced to DCOM, +/-15V are referenced to ACOM
LONA LONB HTR_RTN HTR HTR_SNS SNS_RTN	Unused by Detector PCA
DG_CLK	This is a 60Hz clock generated by smart card. This signal is used to clock the synchronous state machine (implemented within the 7336) that handles HED and CDEM faults.

Table 1:

Signal	Purpose
MS_AB(7:0)	These are the 8 MSE address lines. The following addresses are used by the detector PCA (see the address map for a full discussion of all MSE address assignments): 0: SmartCard reads at this address cause the HED and CDEM status bits to be driven on MS_DB:14,13 respectively. Any writes to this address clear HED or CDEM faults. 6: SmartCard writes to this address to set the fault mask. If the HED or CDEM faults are masked out (MS_DB bits 14 and 13) then the detector PCA will not pull the shutdown line or disable the high voltages when valid faults occur on these devices. 22: Writes to this address enable the CDEM chip select. MSDB:0-11 are latched into the CDEM DAC, and the output level of the CDEM moves accordingly. 35: Reads or writes at this address enable the log amp chip select. Bus contention is avoided because the log amp senses the nMS_WR line and only drives the data bus during reads. 39: Writes to this address cause the detector PCA to latch MS_DB bit 5 (log amp signal channel test). This latched bit is fed to the log amp. When this bit is set, the log amp will provide a triangle wave output. 40,41: Writes to these addresses enable the log amp gain cal chip select. This chip select is sent to the log amp; it allows smart card to re-write log amp gain calibration parameters. 48-63: Reads or writes to these addresses enable the log amp eeprom chip select. This chip select is routed to the log amp. When active, it enables reading and writing of the log amp eeprom. 64: Writes to this address enable the HED chip select. MS_DB:0-11 are latched in the HED DAC, they set the output voltage level.
MS_DB(15:0)	These are the 16 MSE data lines. These lines are routed to the log amp (for ADC reads), are used by the dual DAC (U6), and are used by the fault state machine.
nSHUTDN	This active low line is used by MSE devices to flag a fault and disable the mass spec. The detector board will pull this line low whenever a valid HED or CDEM fault occurs. Activity on this line causes the HED and CDEM supplies to be disabled.

Table 1:

Signal	Purpose
nRESET_MB	This active low line is used to reset all mass spec control circuits. Activity on this line will reset the detector board (all voltages off, all faults/masks cleared).
nMS_WR	This active low line indicates that an MSE write is occurring. The detector board latches incoming data using this line.
n_MS_RD	This active low line indicates that an MSE read is in progress. The detector board will drive data lines when this line is active (assuming the correct address is preset on MS_AB(7:0).

U3 is another dual flip flop. The HED polarity bit and output enable are latched by this part and routed to the supply. The trigger line is CS_HED which is generated by the 7336. This line is clocked whenever HED writes occur. Both flip flops are reset in the event of a system reset or shutdown. This ensures that the HED is disabled whenever a shutdown or reset occurs.

U7 is a dual flip flop used to latch the output enable for the CDEM and the signal channel test line for the log amp. Both triggers are generated by the 7336. Both flip flops are reset whenever a system shutdown or reset occurs.

Hardware External Reference Specification

Document Information:

Filename	**IOERSSP1B.DOC**
Current Owner	**Glen Ingle**
Product Identifier	**G1946B [LC/MSD] [*product revision 1B*]**
Project Identifier	**[Sprite 1B]**
Current Lifecycle Phase	**Investigation**

Revision Log:

Revision	Date	Reason For Update
A.00	**990414**	**Initial revision.** **Instructions: Manually enter the document revisions here and update the corresponding footer revision each time revision log changed. Revision text should include location, time, participants, (R&D, marketing, product support) and a summary of the changes. Also state the revision control system used to recover revisions.**

Executive Summary

See System Requirements Specification Sprite 1B document filename SRSSP1B.DOC.

Functional Description

The I/O Board (IOB) is used to extend the capabilities of the Sprite LC/MSD for fraction collection applications. The IOB accepts up to 3 external analog signals which are the DAD output, a flow detector output, and an additional MS detector. The analog signals are digitized and passed to the SmartCard for data processing in conjunction with the normal LC/MSD data. The IOB provides an analog signal output which is generated by data processed by the Smartcard. This analog signal will be used to trigger external fraction collection devices. The IOB also has 2 digital outputs, one for digital actuation of fraction collectors and the second for general purpose control. Access to the IOB functions is by a 25 pin D sub connector mounted on the left side of the Sprite tub.

The IOB plugs into the Sprite Motherboard and utilizes the MS bus address, data and power interface. The 25 pin D-sub connector mounted in the side of the Sprite Tub wall connects to the I/O board by a shielded 25 conductor flat cable. Control of the D/A converter, A/D converter and the relays is provided by the Smartcard via the MS bus. The I/O board also furnishes a buffered +/- 12 VDC to the 25 pin D Sub connector for powering the Flow Detector module. There is a test connector located at the right top of the board for access to the various voltages present on the Motherboard. There are also 5 LEDs at the top center of the board that visually monitor the Motherboard voltages. There are an additional 3 LEDs immediately below the 25 pin D sub connector for monitoring the status of the IOB. LED 0 is illuminated

The following table lists the various functions available from the I/O board:

Functions		**Description**
Analog Inputs Flow, DAD, Aux	Number	3 Differential
	Resolution	16/24 Bits
	Bandwidth	7.5 Hz
	Input Voltage	-0.1 to 1.0 Volts
	Gain Settings	1,2,4,8,16,32,64,128
Analog Outputs D/A	Number	1
	Type	Voltage
	Configuration	Single Ended
	Resolution	16 Bit
	Bandwidth	DC to 7.5 Hz
	Output Level	0 to 1.1 Volt
	Output Impedance	100Ω
Digital Outputs	Number	2
	Type	Solid State (fraction collect)
		Mechanical (aux)
FC Solid State		
	Form	SPST NO
	DC Contact rating	0.12 Amps @ 400 VDC
	AC Contact rating	0.12 Amps@ 125 VAC
AUX Mechanical		
	Form	SPDT
	DC Contact rating	2 Amps @ 30 VDC
	AC Contact rating	0.5 Amps @ 125 VAC

Architectural Description - Hardware

D/A Converter The D/A converter is controlled by writing 2-16 bit data words to the MS Bus. The first 16 bit word is the output waveform amplitude. The next 16 bit word is the time to delay before outputting the amplitude word to the D/A converter. The time delay is taken to be the time between receiving the time data at the I/O board and the time desired to output the data or control to the external connector. The time delay accumulator is 16 bits; therefore, the maximum count will be 65,536. The delay time increment will be set to 10 milliseconds. The data is accumulated in a circular buffer on the I/O card. The status of the RAM buffer may be checked by reading the write data address.

Fraction Collection Relay The solid state FC relay is controlled similarly as the D/A. The relay state data and the delay time to actuate are sent to specific MS Bus addresses. The buffer

configurations are identical with the D/A ports as well as the read status from both ports. While delayed time relay control is accessed through MS Bus addresses, it is also possible to control the relay directly (bypassing any time delay) by writing a bit to an alternate MS Bus address.

A/D Converter The I/O board A/D converter is capable of monitoring 3 external input signals AUXIN, Flow Detector (FDIN) and DAD. Two internal I/O Board voltages are also monitored for self test purposes which are the D/A output and the 100 mv reference voltage. The 3 external analog inputs are connected through resistor/diode networks to operational amplifiers which buffer the 3 external inputs to the A/D converter inputs AIN1, AIN2, AIN3. The external DAD signal input is, by default, passed through the I/O board without modification although the DAD signal is always connected to AIN3. Actuating the DAD relay connects the DAD signal output to the I/O Board internal D/A converter where analog data may be output by SmartCard. AIN4 always reads the D/A output and AIN5 always reads the internal 100 mV reference voltage.

Mechanical Form C relay A Form C relay is furnished as an general external power controller. The relay is a single coil type and is designated the Aux Relay. It is actuated by writing to a designated MS Bus address. It's status can be read by reading the same MS Bus address.

Architectural Description - Software

The registers in the I/O Board are accessed by SmartCard over the MS Bus. The register addresses span the range of 165 to 176. The following is a list of the functions of the I/O Board arranged by address. The address is shown in hex "**h**" and decimal "**d**" followed by read "**R**" or write "**W**" to that address and a description of the result of the address access.

Address		R/W	Function
A5h	**165d**		**Digital to Analog Converter ~ Amplitude Data ~**
		W	Write 16 bits of Amplitude Data to the Digital to Analog Converter Bits15-0 amplitude data (bit 15 msb)
		R	Reads status of the Digital to Analog Converter Bit0=0 D/A RAM ready Bit0=1 D/A RAM full
A6h	**166d**		**Digital to Analog Converter ~ Elapsed Time Data ~**
		W	Write 16 bits of Time Data to the Digital to Analog Converter. Bits15-0 time data (bit15 msb)
		R	Reads status of the Digital to Analog Converter Bit0=0 D/A RAM ready Bit0=1 D/A RAM full

A7h 167d Fraction Collection Relay ~ Set, Reset ~

W Set/reset the Fraction Collection (FC) relay
Bit0=0 reset FC relay Bit0=1 Set FC relay

R Reads status of the FC relay data RAM
Bit0=0 FC RAM ready Bit0=1 FC RAM full

A8h 168d Fraction Collection Relay ~ Time delay ~

W Write 16 bits of Time Data to the Fraction Collection (FC) relay.
Bits15-0 time data (bit15 msb)

R Reads status of the FC relay time RAM
Bit0=0 FC RAM ready Bit0=1 FC RAM full

A9h 169d Analog to Digital Converter ~ Flow Detect Data (Upper Word)

W Set the channel gain

B3	B1	B0	Gain Setting
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

R Reads data from the A/D
Bits 23 to 8 of 24 bit conversion .

AAh 170d Analog to Digital Converter ~ Flow Detect Data (Lower byte) ~

R Reads data from the A/D
Bits 7 to 0 of 24 bit conversion arranged as low byte of 16 bit word
ie, 00DD. High byte is always 0.

ABh 171d Analog to Digital Converter ~ Aux Input Data (Upper Word) ~

W Set the channel gain

B3	B1	B0	Gain Setting
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

R Reads data from the A/D
Bits 23 to 8 of 24 bit conversion .

ACh 172d Analog to Digital Converter ~ Aux Input Data (Lower byte) ~

R Reads data from the A/D
Bits 7 to 0 of 24 bit conversion arranged as low byte of 16 bit word
ie, XXDD. High byte is always 0.

ACh 172d Digital to Analog Converter ~ Queued data points to delete ~

W n = 16 bit number where n is the number of data points to delete from D/A queue beginning with the data currently being timed. For n equal to or greater than 8000h, the queue is completely cleared. No action if n is greater than the queued data and less than 8000h.

ADh 173d Analog to Digital Converter ~ DAD Input Data (Upper Word)

W Set the channel gain

B3	B1	B0	Gain Setting
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

R Reads data from the A/D
Bits 23 to 8 of 24 bit conversion .

AEh 174d Analog to Digital Converter ~ DAD Input Data (Lower byte) ~

R Reads data from the A/D
Bits 7 to 0 of 24 bit conversion arranged as low byte of 16 bit word
ie, XXDD. High byte is always 0.

AEh 174d Fraction Collection Relay ~ Queued data points to delete ~

W n = 16 bit number where n is the number of data points to delete from FC queue beginning with the data currently being timed. For n equal to or greater than 8000h, the queue is completely cleared. No action if n is greater than the queued data and less than 8000h.

AFh 175d Relay Control and Status: FC, DAD Loop, Aux

W Direct control of the various relays.
Bit 1=0 Auxiliary Relay reset Bit 1=1 Auxiliary Relay set
Bit 2=0 D/A disabled (DAD loop) Bit 2=1 D/A enabled

R Reads status of the Relays
Bit 0=0 FC relay reset Bit 0=1 FC relay set
Bit 1=0 Auxiliary Relay reset Bit 1=1 Auxiliary Relay set
Bit 2=0 D/A disabled (DAD loop) Bit 2=1 D/A enabled

B0h 176d I/O Board ID

R Reads I/O Board ID 16 bit word
E000 = I/O Board Installed
E001 = I/O Board & External Application Box
E002 = I/O Board & External App Box & Flow Detector
E003 = I/O Board in local test.

W word = 1 Set A/D converter for 2 byte (16 bit) conversions.
word = 2 Set A/D converter for 3 byte (24 bit) conversions.
word = 3 Turn on the Flow detector LED for calibration.
word = 4 Turn off the Flow detector LED.

Motherboard Connector J1 Pin Assignments 96 pin DIN (F)

Pin /Col	A	B	C
1	NC	+24VDC	+24VDC
2	NC	+24VDC	+24VDC
3	ACOM	LONA	LONB
4	ACOM	ACOM	ACOM
5	+15VDC	+15VDC	+15VDC
6	+15VDC	+15VDC	+15VDC
7	-15VDC	-15VDC	-15VDC
8	ACOM	ACOM	ACOM
9	VCC	VCC	VCC
10	VCC	VCC	VCC
11	VCC	VCC	VCC
12	DCOM	DCOM	DCOM
13	DCOM	HTR_SNS	SNS_RTN
14	DCOM	DCOM	DCOM
15	HTR_RTN	HTR_RTN	HTR_RTN
16	HTR	HTR	HTR
17	DCOM	DCOM	DCOM
18	DCOM	NC	DG_CLK
19	DCOM	MS_AD1	MS_AD0
20	DCOM	MS_AD3	MS_AD2
21	DCOM	MS_AD5	MS_AD4
22	DCOM	MS_AD7	MS_AD6
23	DCOM	MS_DB15	MS_DB14
24	DCOM	MS_DB13	MS_DB12
25	DCOM	MS_DB11	MS_DB10
26	DCOM	MS_DB9	MS_DB8
27	DCOM	MS_DB7	MS_DB6
28	DCOM	MS_DB5	MS_DB4
29	DCOM	MS_DB3	MS_DB2
30	DCOM	MS_DB1	MS_DB0
31	DCOM	nRESET_MB	nSHUTDN
32	DCOM	nMS_RD	nMS_WR

Test Connector P1 Pin Assignments 2x10, 20 Pin .100” Header (M)

Pin /Col	A	B
1	DCOM	AN1
2	nRESET_MB	AUXRLY_STAT
3	ACOM	DADRLY_STAT
4	+15V	FCRLY_STAT
5	ACOM	ET_TICK
6	-15V	TESTC
7	VCC	AN3
8	ACOM	DTA_OUT
9	+24V	NC
10	nSHUTDN	AN2

Application Connector J2 Pin Assignments **25 Pin D-Sub (F)**

Pin	Function
1	ACOM
2	Flow Detector -Input
3	Auxiliary +Input
4	ACOM
5	DAD -Input
6	DAD +Input
7	ACOM
8	DAD –Input ~ D/A Output Return*
9	TESTC (flow det LED)
10	FC Relay Contact 1
11	XAPP1
12	Aux Relay Contact Common
13	XAPP2
14	Flow Detector +Input
15	ACOM
16	Auxiliary -Input
17	DAD +Input
18	ACOM
19	DAD -Input
20	DAD +Input ~ D/A Output*
21	+12VDC
22	-12VDC
23	FC Relay Contact 2
24	Aux Relay Contact NC
25	Aux Relay Contact NO
** Loop relay state controls connection*	

Compatibility With Other Products

This device is compatible with all models of Sprite, although the functions may not be accessible without the necessary Fraction Collection system software.

Product Options

There are no internal options supported by the I/O Board. However, the I/O Board supports an external applications interface box including the Fraction Collection Flow Detector.

Customer Setup and Configuration

Not customer installable

Performance Specifications

See function Description and specifications above.

Serviceability

There are no User serviceable components on the IOB. Boards must be returned to a proper repair facility in the event of problems.

Testability and Error Handling

The I/O Board has on board diagnostics that function on power up. LED's located near the top left of the board indicate normal and test operations. The state of the LED's indicate a detected fault which can be traced to the functional component level.

A test connector has been included on the IOB to provide monitoring of the Sprite internal Voltages as well as the I/O board functions.

Appendices—Open Issues

The IOB software and some functions may require modification as Fraction Collection methods are developed.

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REV	REVISIONS	APPROVED	DATE
A	AS ISSUED PER PC23-6257	B. MELANSON	01/08/98

James Bertsch DRAWN BY	01/08/98	**DESOLVATION ASSEMBLY THEORY OF OPERATION** TITLE	HEWLETT PACKARD
James Bertsch ENGINEER	01/08/98		
Bill Melanson RELEASE TO PROD.	01/08/98		G1946-60036 PART NUMBER
SUPERSEDES DWG.	CURRENT REV A	PAGE 1 OF 7	**A-G1946-60036-2**

Desolvation theory of operation for the G1946A

This document is intended for LC/MSD manufacturing engineers or R&D engineers and is not appropriate for other distribution.

Please refer to G1946-60036 assembly drawings. These notes are dated 1/4/98 and will not be updated.

The desolvation assembly acts as the interface between the nebulizer and the first skimmer. It's primary purpose is to dry the droplets (mostly in the spray chamber), and transport the Ions up a potential gradient and into the first vacuum stage.

End plate:

Carries the high voltage which causes charged droplet formation from nebulizer. Was made easily removable late in the project. Has interesting bug/feature: If end cap is tightened with m3 screws loose and the the m3 screws are tightened, the nut flexes and the end cap is locked in place. If only one of the screws is tightened and the end cap is untightened a quarter turn before the second screw is tightened, then the end cap becomes customer removable without a tool. This is what is done on the manufacturing line. The auxiliary gas hole in the cap was added also at the end of the project. It blows a little high temperature nitrogen across the end of the nebulizer, establishing a low relative humidity. This prevents condensation on the needle and resulting drips (and signal dropouts) even at high (1-2 ml/min.) flows. It serves no purpose at low flows but doesn't appear to cause any problems either. This "defroster" action is really the only reason the hole needs to be oriented "up". The endplate is 316 SS as are most of the steel parts in the spray chamber. 304 is not good enough and will discolor. We are considering changing the screws to 316 also.

Spray Chamber Mount:

Machined aluminum: good surface finish. Thought about die-casting or other techniques but did not pursue them. This part, like the spray chamber itself, is plated with nickel and then Rhodium. Just nickel plated is no good. It will turn black. We are not sure why, but the surface science test results indicated carbon buildup which could be some catalytic reaction dependent on solvent composition etc. Bare aluminum would be a cosmetic problem and will corrode where the spray hits it. It might be a charging problem also. The rhodium, although thin, is far superior to anything we have seen. Unfortunately, it makes the parts not reworkable because the plating shop (was HP Santa Rosa) can't get it off once it is on without destroying the aluminum. 316 SS would also work of course, but would probably triple the cost. The spray chamber mount is rather carefully designed to drain well without big puddles, and while keeping the O-Ring seal dry.

Spray chamber high voltage cable:

The spray chamber high voltage cable was originally 30kv Teflon cable. Now it is 20KV rated to allow a better strain relief at the multicontact gold connectors. These connectors lose temper at about 181C according to Multicontact, but our tests indicated that even worst case (ambient, drying gas load, etc.) we still have more than 10C margin.

T-Nuts:

pins should also be 316 but aren't yet. Customer support wants a unique T-nut on the right without a pin to avoid the possibility of misconnecting the center wire (actually happened once in the field). They are rounded to avoid creating Teflon slivers when installed.

Interlocks:

The slots in the endplate mount and were narrowed and the extra lip on top was added by Tor to solve a potential safety issue involving the 4MM diameter vertical probe, and the worst case hysterisis in the magnetic interlocks. We are probably being overly cautious, but why not. The magnetic switches are IEEE approved for use as a single fault safety interlock. Most magnetic switches are not. Only the outer one is actually a safety interlock. The inner one merely identifies which spray chamber is attached. Don't monkey with the geometry without considering the worst case high voltage turnoff finger clearance.

Capillary:

Problematic part. The plating by AOB wears off. It is about ten millionths of an inch of platinum. It is painted on and baked and the adhesion is terrible. It tends to wear off at the corners. However, the capillary still seems to work as long as there is electrical continuity to the face. We have had charging problems which manifest themselves as a drop in signal level especially at the low masses. We have tried painted on gold. It doesn't stick very well either. Using the sand blaster downstairs to rough up the surface before painting with the gold looks marginal but actually works better. The plating still wears off but continuity appears to be maintained because of the surface roughness. Recently we have started trying some deposition ideas. We hope to get better adhesion, achieve a thicker layer, and top it off with some rhodium which has proven to be outstanding with respect to chemical resistance and also has excellent hardness. The capillary procurement is wrapped up in the intellectual property deal with AOB. We were initially going to use a new AOB source, but their inability to deliver a prototype caused us to accelerate our own developments. The capillary is the only remaining AOB supplied part (they insisted), and is probably the biggest warranty problem. The high temperature at the entrance end seems to exacerbate the adhesion problem for the plating. For this reason and also to avoid contaminating the capillaries (unverified effect), the 400C 15 lpm bake-out of the desolvation assembly is done with a dummy capillary.

Capillary Caps:

they aggravate the plating problem because the canted coil springs wear the plating off. The springs used to be stainless steel unplated and with a lower spring rate. This was fine for electrical contact, but was a little loose for the front cap because it tended to slide off too easily. Switching to gold plating was primarily for cosmetic reasons to distinguish from the earlier parts and was thought to lead to less wear. This may not be true at all. The wear is made worse by the canted coil spring dimensional change at high temperature, which is about 6% diameter change when the spring temperature is raised to around 250C as it is in the source during operation. This was measured (to their great surprise) by the manufacturer. We tried a hastalloy spring which was only a little better. It appears to be a one time only stress relaxation effect, but it does tend to increase the plating wear

problem. The capillary caps are the same on both ends of the capillary primarily for DFA and cost. The chamfer on the exit end is very important. Without it some strange shock wave effect occurs which causes the stage four pressure to be abnormally high, and the resulting problem can't be easily solved by increasing the capillary skimmer spacing. It may be that the diameter increase and the web thickness is such that we get a crude supersonic expansion nozzle without the chamfer. I don't know. The chamfer doesn't seem to make a big difference on the front end. The I.D. of the through hole is a balance between trying to cover up as much of the capillary as possible on the front ends as possible while not messing up the mach one expansion at the exit. The cap in front wobbles a little because the design width is based on the old lower spring rate spring. It should be narrowed. See Karl Horstmann for info. During development, a number of ideas were tried for caps, such as kovar caps cemented on with silver loaded conductive cement. It was very messy. A removable front cap is desired by many chemists because they find it very easy to clean. The front cap was originally though necessary to avoid blowing off the plating with arcs. With our fixed front geometry and with our fixed 500 volt differential, this is probably no longer the case as it was with Engine. Having the front cap is still preferred by Steve because of the above mentioned cleaning issue and also because he says that some of the chlorinated solvent systems will strip the platinum off the capillary, and he wants to reduce the exposure of the capillary to a minimum. The exit cap is required because it acts as a mechanical stop to set the capillary-skimmer distance. The assumption is that the capillary is pushed in all the way when it is inserted (it will stay there because of bal-seal friction). Attempt was made earlier in the project to have the friction forces of the bal-seals low enough that the vacuum pressure on the cross sectional area of the capillary would be enough to guarantee that the capillary would be in all the way, but there really isn't enough force to work with.

Capillary-Skimmer distance:

Important, it establishes the downstream pressures. Making this distance fixed, and precise, and achieving coaxial alignment, while not requiring the user to adjust anything and while allowing the user to easily separate them for cleaning, was a key product definition item. There are relatively few dimensional tolerances which add up, and these are the tightly controlled dimensions on the prints. See Kent s notebook for test data relating to capillary-skimmer spacing. This distance working with the voltage gradient also establishes the conditions for fragmentation. Fragmentation can also occur between skimmer1 and skimmer2 but we found late in the project that linking the voltage of S1 to be a fraction of the Capillary to S2 voltage can avoid this undesirable effect for most molecules.

Exit insulators:

They used to be simple washers but we had fragmenter fault problems. I am not certain that we are using the best material for these parts. Teflon might be another choice because of it s electrical properties, although the dimensional stability isn't the greatest. The fragmenter faults are relatively rare since the surface creepage distances were increased and seem to be related to cleanliness concerns because when they do occur they can be fixed by cleaning the parts. This problem only seems to happen close to the 400 volt limit and I have always had to go higher that that to initiate the problem. A consultation of the passion curve will show what a sensitive area vacuum stage one is for arcing. This concern was one of the motivating factors for the current design which uses the capillary itself as the feedthrough and avoids making electrical contacts in stage 1. Keeping the insulators out of the line of sight of the ion stream is also a concern. One of the insulators contributes to cap-skimmer

spacing, the other spacer contributes to cap-skimmer concentricity.

Drying gas heater:

Leveraged from 5972 transfer line but higher wattage in order to guarantee 13.5 lpm and 365C under all line voltage conditions. Tolerance on diameter is important.

Drying gas sensor:

Used on GC/MSD and GC s. Really inexpensive. Be cautious changing this part as its internal thermal conductivity and the location of the temperature sensing element inside it are part of the control loop, and there is a larger end to end temperature gradient in the DG heater body. It is not specified to work above 450C and I have seen it fail earlier in the project because of thermal runaways (not necessarily a bad thing because the heater shuts off).

Drying gas assembly:

This evolved from a design where the heater body was aluminum. The truncated acme thread and the small diametric clearance above each fin was designed to give the minimum delta T between the heater body and the gas so as to allow a large swage lock fittings to be used to seal the steel outer tube to the inner heater manifold body. During one thermal runaway during the LP phase we actually exceeded 650C in the heater body and the aluminum melted. The instrument still worked (nothing caught fire) but the absence of drying gas and thermal decomposition particulates in the source did have a negative effect on instrument performance. To make it more bullet proof we switched to an all stainless welded design. Although that precludes us from effectively cleaning the inside surfaces of the heater assembly after welding, the bake out/ blow out procedure seems to be effective coupled with the pre welding cleaning notes. Because the Delta T is no longer so critical with the all stainless design,it might be possible to simplify the helical air path and save a little money. The exit end of the heater body is much hotter than the inlet end because of the low thermal conductivity of the stainless, and the sensor is really measuring some kind of average. At the exit end there is a double wall construction to decrease the conductive path to the mounting point and to the bal-seal, and to maintain the gas temperature at its high level. The diameter of the heater was kept small and it is tilted to keep the O.D. which is ground away from the capillary.

Drying Gas Insulation:

Shaped on outside to discourage placement of the tape on the hottest surface (where it would discolor) and to give access to the mounting screw. Steel cable ties were tried instead of tape but were a mess.

Drying Gas Path:

The gas volumetric flow rate is adjustable from about 3 to 13.5 liters per minute. It does not have much specific heat and consequently cools rapidly as it finds its way past cooler structures to the end cap. Ideally the heater would be in the end plate, but since this is at 2-7 kilovolts the heater is done remotely .

Maximum Drying Gas Temperature:

The limit used to be the Teflon directly across from the heater which slowly decompose and turn black at about 350C and 15 lpm. However, the Teflon material was changed, the clearance was increased, and a little baffle was added to the heater exit to redirect the flow downward to decrease the surface temperature of the Teflon. The maximum setpoint is 350C for APCI and 365 for Electropsray. It is possible that a full 400C would be OK but extensive testing would be required to verify this.

Baffle and Vcap Spacer:

Vespel. Tried Torlon, it charred. Teflon would probably mush and decompose. The baffle seems superfluous but it stops the cavity from whistling and evens out the gas distribution. Forgetting to install it has caused high mass instability in the past on some instruments. The Vcap spacer spaces the two voltage elements and keeps the gas flowing smoothly without excessive turbulence.

Endplate mount:

Modified (PPV) teflon, see print. Process info is important to avoid trapped gases. This complicated part creates the gas path, aligns the capillary and the end cap, holds off 7kv capillary and 6.5kv endplate voltages from ground, acts as thermal insulation, holds the electrical contacts etc. It has to withstand high temperature yet have low thermal conductivity. It must have very low electrical conductivity and extremely high chemical resistance.

Material alternatives:

We used to use Teflon with 25% glass filling but that has reduced temperature stability, increased affinity to amines, and potential fiber/particulate noise problems. Machineable ceramic was tried once but the electrical conductivity was too high at elevated temperature and it was too brittle. High purity alumina might work but would be very expensive. Vespel is also a maybe but also has a high cost implication. The complicated steps on the outside are to decrease the possibility of making a surface conduction path in the wet spray chamber environment.

Assembly design intent:

To have a self aligning design. I.E. no assembly fixturing or adjustments.

Cleaning Design Intent:

Easiest access to end cap and capillary cap for frequent cleaning depending on customer loading. Capillary removable and cleanable without tools. Front of Skimmer one easily accessible for cleaning without changing source alignments or removing top cover of instrument.

Assembly notes:

Although the desolvation assembly can be removed from the instrument intact, the desolvation assembly should not be take apart without first pulling out the capillary.

Interlocks:

The interlocks are carried in the same cable assembly as the high voltage so that the high voltage is disabled when the connectors are disconnected.

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REV	REVISIONS	APPROVED	DATE
A	AS ISSUED PER EC23-70090	K. Horstman	07/30/98

Gerson Goldberg DRAWN BY	01/12/98	**FLOW CONTROL ASSY THEORY OF OPERATION** TITLE	HEWLETT PACKARD
Michael Flanagan ENGINEER	01/12/98		
Karl Horstman RELEASE TO PROD.	07/30/98		G1946-60038 PART NUMBER
SUPERSEDES DWG.	CURRENT REV A	PAGE 1 OF 9	**A-G1946-60038-2**

General Hardware Description:

The Flow Control Module provides dry nitrogen flow control for three instrument subsystems:

Counter Current Drying Gas
Nebulizing Gas
CDS Head Pressure/Line Purge Gas

Both the drying gas and nebulizer gas use similar hardware and control mechanisms. Each channel consists of a solenoid proportional valve, pressure transducer, and flow restriction orifice.

Control Mechanism:

The feedback control for the gas flow controller is provided by the PDB PCA (G1946-60002). The control constants are contained in the firmware on that board. The gas flow control assembly is actually a pressure control device. Flow is "controlled" by controlling the pressure upstream from a fixed restriction. Therefore, the flow accuracy is subject to changes in temperature and restriction geometry. The pressure upstream of the restrictor is varied by adjusting the upstream flow through a solenoid proportional valve. Pressure readings are read back by the control logic and the PWM duty cycle is adjusted in order to open or close the valve, thus compensating towards the target pressure.

Solenoid Proportional Valve:

The same Pneutronics solenoid proportional valve is used for both the drying gas and nebulizing gas control channels. The orifice in the valve measures .030" and the valve seat material is viton. Flow rate is adjusted by flowing an appropriate current through the coil, effectively increasing the leak rate past the valve seat through the orifice. The current is adjusted through regulating the delivered voltage, actually controlled by a pulse width modulated drive from the Power Distribution Board. It should be noted that a similar valve was used in the 6890 Gas Chromatograph in the Electronic Pressure Control system.

Initially, severe stability problems were experienced with these valves. The problem turned out to be the bonding agent used to adhere the valve seat to the internal components. As the valve would heat up (due to being energized), the bonding agent beneath the valve seat would cause the valve seat to bulge and partially obstruct the flow through the valve. Eventually, the system would be unable to compensate for the increasing restriction and maximum required flow rate could not be achieved. The bonding agent was changed to ChemLok which completely resolved the problem. Flow rates up to 16 liters/minute are obtainable with an 80 psig supply pressure. This flow rate is software limited to 13 liters/min in order to ensure proper margin.

Pressure Transducer:

The pressure transducer is a key element of the feedback control circuit for controlling the flow of the nebulizer and drying gases. The pressure of the gas upstream of the flow control orifice is measured by independent Sen-Sym ST2000 pressure transducers. The amplified analog output of the sensor is readback by the Power Distribution PCA and the Solenoid Proportional Valve is adjusted appropriately.

Due to the design of the sensors, the SenSym transducer provides a contamination free fluid path because it is sealed from the fill oil and pressure sensing integrated circuit via a stainless steel diaphragm. This allows the sensor to be compatible with any material compatible with 303 stainless steel.

Flow Restriction Orifice:

The Drying Gas flow restriction orifice is built in to the drying gas outlet of the manifold itself. The exit hole is drilled to precise tolerances which should give no greater than a 10% flow error at worst case at 50psi. Alternatives to the drilled orifice are precision drilled press in orifices or stainless steel frit orifices. Both of these solutions could provide more consistent flow from module to module at the expense of increased part cost. The cost of the press in restrictors can be as high as $20 each.

Since the user actually sets drying gas flow rate and only pressure is measured, it is extremely important that the orifice be of consistent diameter so there is not significant instrument to instrument variation. The relationship between pressure and flow rate must remain consistent among all instruments since the drying gas flow rate is a typical method parameter which may be adjusted due to differences in mobile phase composition, flow rate, and sample type.

Whereas the drying gas flow rate is controlled by an integrated restriction, the nebulizing gas flow is restricted by the nebulizer itself. Therefore, if the nebulizer is not connected to the nebulizer gas output, the gas flow system will not be able to supply sufficient nitrogen flow in worst case situations.

In both situations, the orifice back pressure or downstream pressure is assumed to be constant from instrument to instrument. This is an accurate assumption for the nebulizer gas since it exits to the spray chamber which should be atmospheric pressure. Therefore, all other components being equal, flow rate could be altered by changes in atmospheric pressure in spray chamber (ie due to altitude, temperature, waste vent vacuum, etc.)

On the other hand, the drying gas flow rate is subject to restriction differences in the heater and drying gas flow path (which eventually empties to the spray chamber.) Therefore, desolvation assemblies are checked for abnormal flow restriction so as to make certain that the flow is not overly restricted.

CDS Relief Valve / Regulator:

The CDS Pressure Relief Valve is installed to protect the user and system from overpressuring the glass calibrant bottles shipped on the system. The relief valve will release gas when the regulator output pressure exceeds the set pressure on the valve (near 15 psi), preventing the bottles from exploding under excessive gas pressure.

The regulator adjustment is not a user serviceable adjustment nor is it an operating parameter. The pressure is factory set at HP to 13 psig and requires both a tool and removal of two levels of covers to access.

The CDS head pressure has been iterated to provide sufficient sweeping of the lines to avoid air bubbles in the calibrant delivery lines. For more information on these studies, please refer to the CDS Theory of Operation.

Flow Control Assembly Relief Valve:

A flow control assembly pressure relief valve (100 psig) is installed to protect the assembly from overpressurization. Overpressurization of the assembly could lead to damage to the proportional valves, pressure regulator, and pressure transducers.

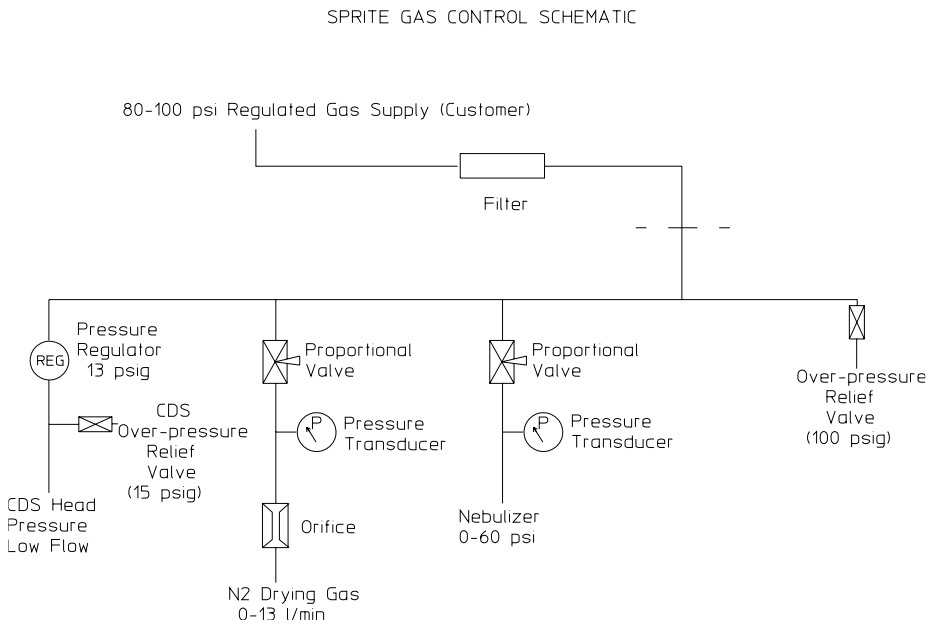
Gas Purifier/Filter:

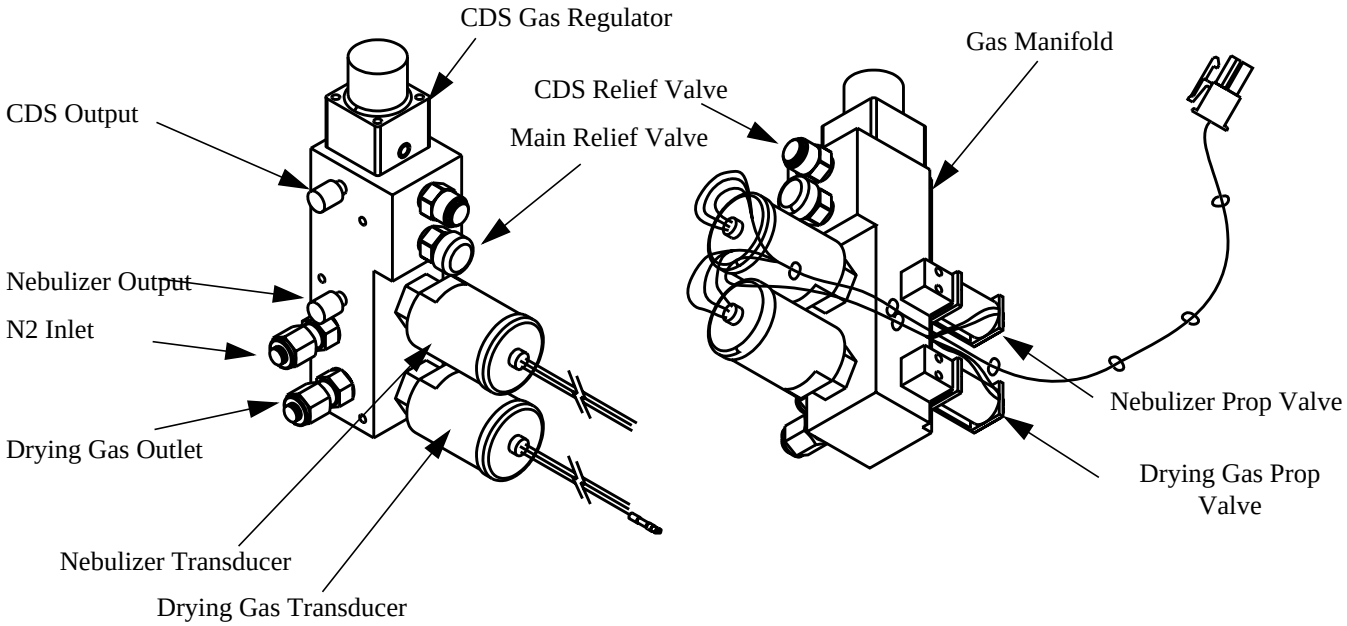
A zeolite gas purifier containing a 10mm filter is located just upstream of the flow control assembly. The purifier removes organic contaminants and particulates from the nitrogen supply gas. The filter is installed outside of the instrument between the supply tank and the nitrogen inlet on the instrument.

Material Choices:

All materials in the flow path have been chosen to be compatible with the MS system so as to avoid any sort of contamination. The aluminum manifold body is clear anodized to help reduce reactivity with the aluminum. The inert properties of teflon tubing again provides an inert path for the gas to follow. As mentioned earlier, the pressure transducers are constructed such that the gas only comes in contact with 303 stainless which is not as chemically inert as 316 but should suffice since those parts are not coming in contact with solvent or sample.

SYSTEM SCHEMATIC





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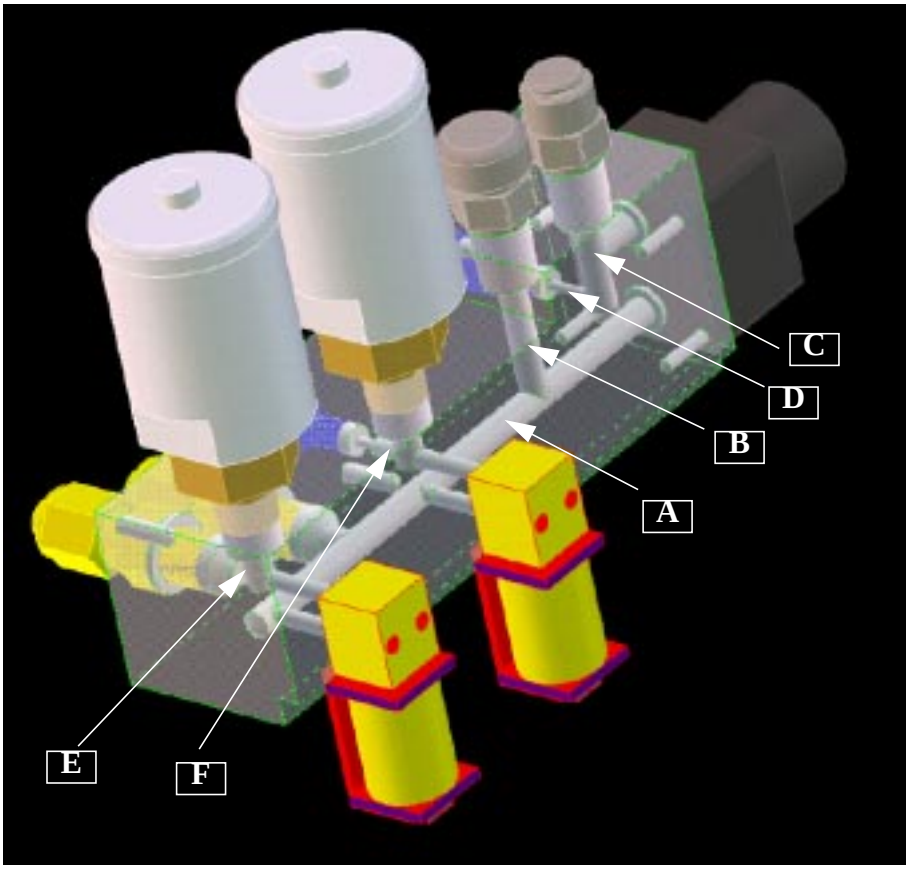
MANIFOLD PLUMBING

The following graphics show the internal plumbing inside of the Gas Flow Control Assembly. The legend below shows the different plumbing channels within the manifold. The walls of the manifold have been made transparent in the graphic so as to show the internal channels. These are not visible on the actual part.

Pointer	Description
A	Main Pressure Channel
B	Main Pressure Relief Channel
C	CDS Relief Channel
D	CDS Outlet
E	Drying Gas Outlet (pressure)
F	Nebulizer Gas Outlet (pressure)



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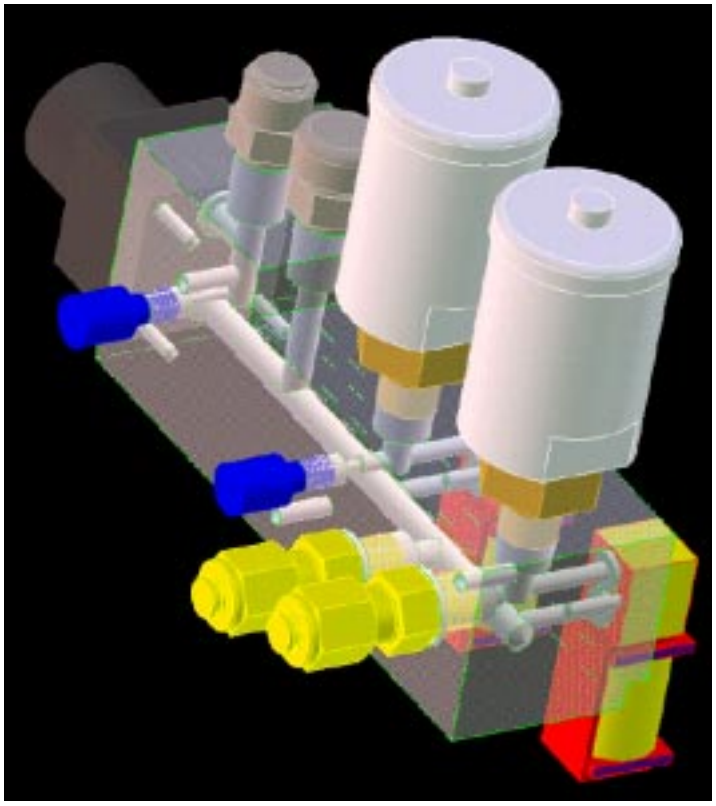

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SMART CARD FLOW CALIBRATION FUNCTIONS

The following polynomial functions are embedded in the SmartCard firmware to convert flow rates to pressure and visa versa. The system needs to convert flow rate to pressure in order to set the flow while the system must be able to convert pressure to flow rate in order to report back the actual flow rate to the user.

p: pressure (psig)
f: flow rate (SLPM N2)

$p <= 0$ -> $f = 0$
$p < 10$ -> $f = C_{00} + C_{01} * p + C_{02} * p^2$
$p < 50.05$ -> $f = C_{10} + C_{11} * p$
$p > 50.05$ -> $f = 13.5$

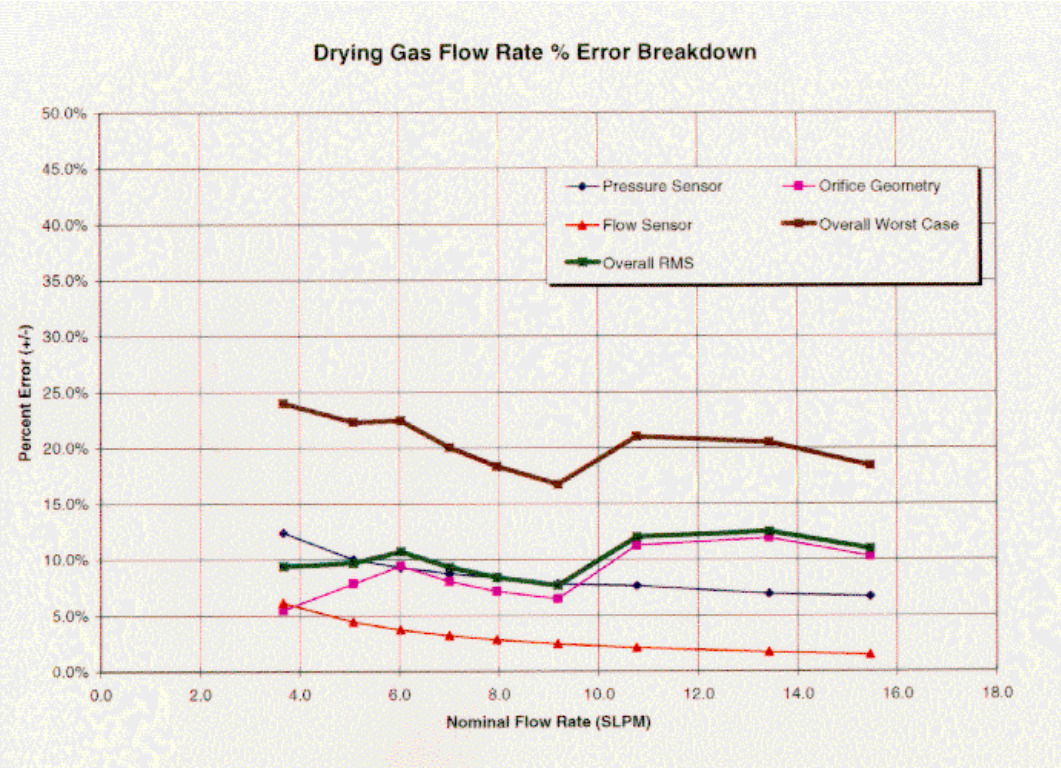
$C_{00} = 0.1216780926894403$
$C_{01} = 0.6516182177507226$
$C_{02} = -0.0218583358280659$
$C_{10} = 2.33$
$C_{11} = 0.223$

UNCERTAINTY ANALYSIS

An uncertainty analysis was performed based on the tolerances of the following components
- Orifice Size
- Pressure Transducer Accuracy
- Calibration Flow meter accuracy

While the Calibration Flow Meter is not part of the device, it was used to create the initial calibration functions as well as being used to measure the flow in the subassembly pretest. The plot below shows the results of the uncertainty analysis for both worst case and RSS error analysis. The test specifications have been chosen based upon the RSS values as it was decided by the design engineers that the worst case specifications would be too loose. These specifications are not detailed here as they are kept in the manufacturing test software and may be changed without reference to this document.

This type of specification setting has not proven to be bullet proof. In fact, there have been significant failure levels due to too narrow a specification margin. Experimental data should be collected to verify the individual component uncertainties.



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REV	REVISIONS	APPROVED	DATE
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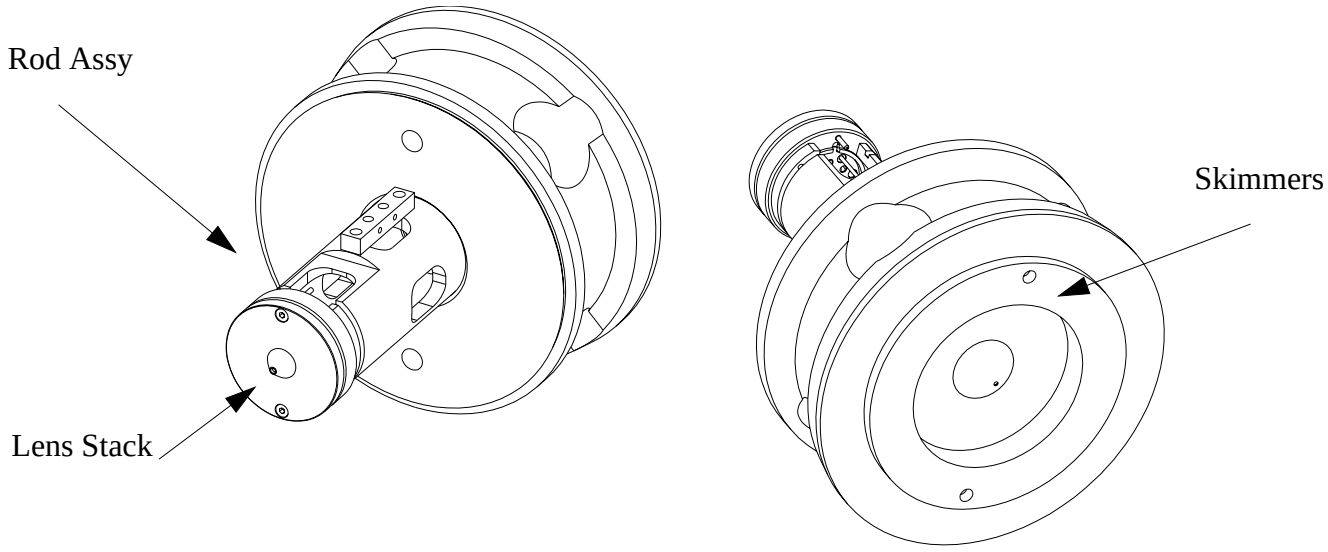
Theory of Operation

Please note that this document does not include any specific dimensions as it is not intended to provide any detailed specifications. This document is intended to provide a general understanding of the design and operation of the assembly. In addition, this document describes some of the problems experienced during development as well as some suggestions for improving the design that were not incorporated due to project time or scope. It is our intent that this document need not be revised when minor changes are made to parts without intended changes in function.

Overall Assembly Theory of Operation

The Octopole Assembly (G1946-60041) serves many functions. In fact, the name is somewhat misleading because the "Octopole" portion of the assembly performs only part of the functionality of the assembly. The assembly consists of three major regions, the skimmers, rod assembly, and lens assembly. Below is a brief description of the functions of each stage. A more detailed discussion of each stage follows.



The first section is the skimmer section which acts as a momentum separator for the incoming sample vapor. It is important to remember that the capillary is sampling a combination of neutral drying gas and solvent molecules and analyte ions. This assembly helps to pump away the low momentum solvent and drying gas molecules and transmits the higher momentum analyte molecules. In addition, the skimmer orifices provide the conductance limits between stages 1 and 2 and stages 2 and 3. These conductance limits are established so as to limit the gas load into the high vacuum stages.

The second section of the octopole assembly is the actual rod assembly (from which the assembly gets its name.)

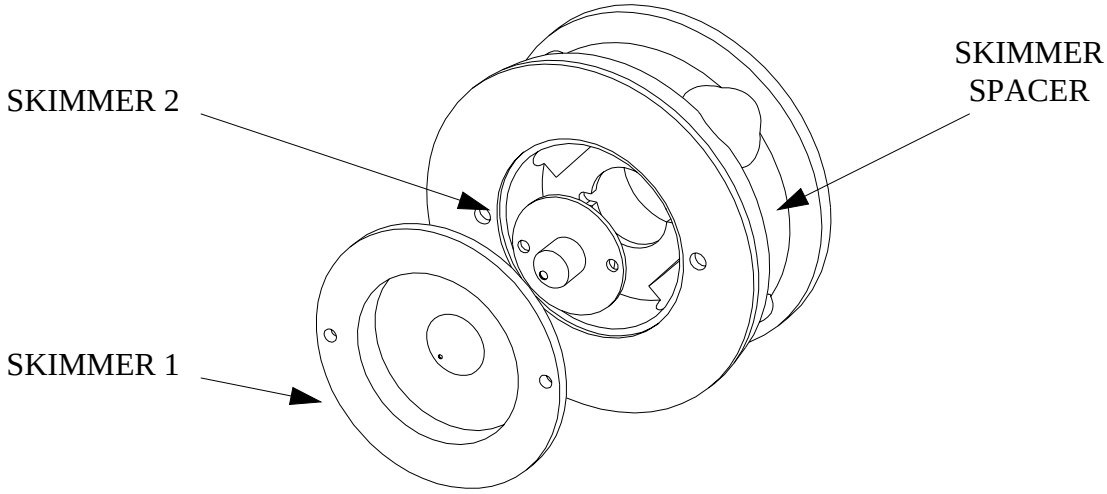
The rod assembly serves multiple functions. Primarily, it acts as an ion beam guide which columnates the ions and transmits them to the quadrupole entrance. This effect is achieved through the application of both an AC and DC voltage on the rods. The second major function of the rod assembly is to control the energy of the ions entering the quadrupole, thus providing for better resolution in the mass filter. This effect is controlled by the DC offset on the octopole rods as well as control of the viscous/molecular flow transition which occurs along the axis of the rod assembly. The location of this transition defines where the ions' kinetic energies are no longer influenced by collisions but solely by electrostatic forces. This allows for a narrow band of ion energies entering the quadrupole.

The final section of the assembly is the lens assembly which consists of two sequential electrostatic lenses. The primary functions of the lens stack is to establish an electric field gradient which pulls the ions out of the octopole rods and injects them into the quadrupole. Another important function of the lenses is to shield the ions from the fringe fields of both the octopole and quadrupole rod ends.

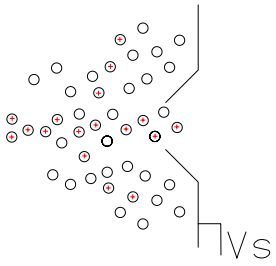
Finally, the lenses also provided a conductance limit between stage 3 and stage 4 of the vacuum system. The orifice size is critical in reducing the gas load on stage 4, essential for proper function of the quadrupole mass analyzer.

Momentum Separator Theory of Operation

As stated earlier, the skimmers in the momentum separator are designed to "skim off" the low momentum solvent molecules. It is important to remember that the capillary samples both charged analyte ions as well as neutral gas (primarily Nitrogen) and solvent molecules from the mist delivered by the nebulizer. The assembly is actually a two stage momentum separator which helps to eliminate lighter neutral molecules from entering downstream vacuum stages. This reduces the load on the downstream vacuum stages allowing the instrument to reach critical vacuum pressures needed to analyze the mass to charge ratio of the sample ions.



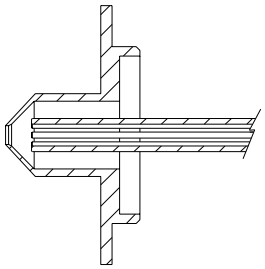
In order to improve ion transmission through the skimmers, a DC voltage is applied to the skimmers so as to maintain the ion beam exiting from the capillary. As the neutral gas expands due to the pressure reduction, the gas molecules would tend to knock the ions out of the center beam without the influence of an electrostatic field. The generated field provides a restoring force to the ions to push them back towards the center after being knocked off course by the escaping neutral molecules. The polarity of the skimmers is always the same as the ion. The graphic below shows some ions being knocked off center as the neutral gas molecules expand away from the center and are "skimmed" off.



In order to control the gas load into downstream vacuum stages, the orifice diameters are chosen so as to help

achieve the proper pressures needed for analysis. There is a trade-off, however, between ion transmission and the orifice size. Therefore, the orifice diameter has been optimized to transmit the greatest number of ions without allowing the downstream pressures from rising too high. It is important to know that changes in these diameters should not be made without understanding the relationship between diameter, pressures, and ion transmission.

The skimmer angles are designed such that the low momentum molecules are steered away from the high momentum molecules and toward the vacuum inlet. The skimmer spacer maintains the distance between the spacers as well as provides a conductance path for stage 2 pumpout. Again, alterations to this spacing will result in changes in pumping efficiency within the stage and may result in averse downstream pressure effects. The angle of skimmer 2 is also designed to accommodate the octopole rod assembly which must meet up closely to the skimmer exit. This angle was chosen given the OD of the rod assembly and the proximity needed for efficient ion transmission. It is important to note that a design improvement would be to have the octopole assembly pass through skimmer 2, however, this design is currently patent protected by HP competitors.



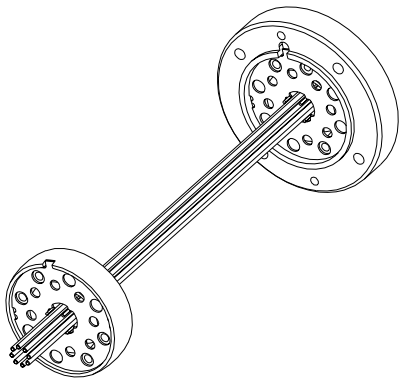
The skimmers are mounted with Oring seals. The oring around Skimmer 1 is a viscous flow seal from stage 1 to stage 2. In addition, the seal on the outside of the skimmer spacer provides a viscous flow seal from stage 1 to stage 3. This seal is between the skimmer spacer and the vacuum chamber. Finally, Skimmer 2 does provide a seal between Stage 2 and Stage 3. In this situation, since the pressure differential is not as great as in the previous instances, a hermetic seal is not established. An optical baffle is sufficient to maintain the pressure differential between stages 2 and 3. Therefore, the conductance between stages 2 and 3 is subject to gross variations in fit between Skimmer 2 and the Skimmer Spacer. This has not shown to be a problem.

Design Notes:

Material Selection:

Both Skimmer 1 and Skimmer 2 are made from 6061-T6 aluminum which is electroless nickel plated. The primary purpose is to prevent oxidation of the electrode. Since the skimmers do setup an electrostatic field to contain the ions, non-conducting surfaces could develop uncontrolled charges and cause unwanted distortions in the electric field. This could affect overall ion transmission. Furthermore, the nickel coating is much more inert than the aluminum which would likely react with the samples or solvents sent through the skimmers. The nickel acts as a chemical boundary between the input sample and the aluminum.

The reason why the skimmers are not made of stainless steel is primarily for cost and machinability. The skimmers have very fine points and thin wall sections. This proved very difficult to machine in 316 stainless steel. Therefore, nickel plated aluminum was chosen for simplicity of manufacturing.



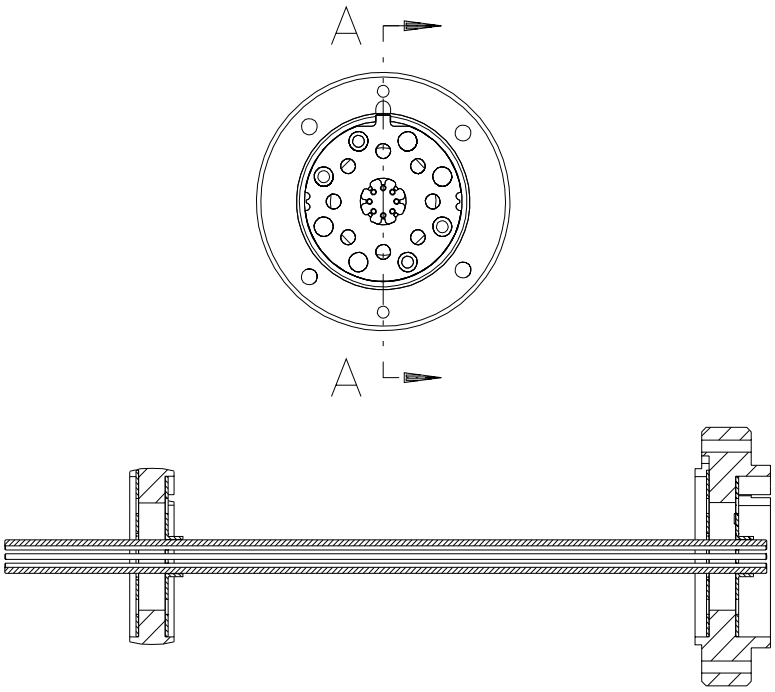
The octopole rod assembly performs a number of functions. One function of the octopole is to columnate the ion beam and transmit it into the quadrupole. This effect is achieved by the application of an RF voltage on the rods which are 180 degrees out of phase between adjacent rods. This change in radial potential causes the ions columnate as they continue through the ID of the rods. This setup creates a high pass mass filter which rejects low mass ions. Whereas the quadrupole fields are designed to create a very narrow band pass filter, the fields generated inside the octopole are designed to allow a much broader band of high mass ions (when the RF is set to the maximum setting.) In order to compensate for this high mass discrimination, the RF voltage is ramped to its maximum through the low mass region. The reduced RF voltage shifts the filter down the mass axis, thus transmitting the low mass ions. This ramp is performed on every scan. (For more information, please refer to the Theory of Operation and Engineering Report for the Octopole Drive PCA G1946-60009.)

The internal diameter or 2R0 is specified to tighten the beam diameter. By having a tighter beam diameter, the ion density is increased. Since the ions sampled by the quadrupole are only admitted through a very small acceptance aperture (approximately 0.1 mm in diameter), the increased density increases the overall ion transmission through the quadrupole and thus helps to increase instrument sensitivity. The 2R0 of the octopole rod assembly is limited on the low end by a few factors. One such limit is the need for vacuum conductance into the central region. Given the rod diameter, if the R0 were to be reduced too much, the conductance would be too low and the region of the ion beam would not be able to reach sufficiently low pressures. Another limit is the need for a large enough beam such that the it is much greater in diameter than the acceptance aperture. If the beam were to be near the same diameter as the acceptance aperture, the alignment between the octopole assembly and the quadrupole assembly would have to be much tighter.

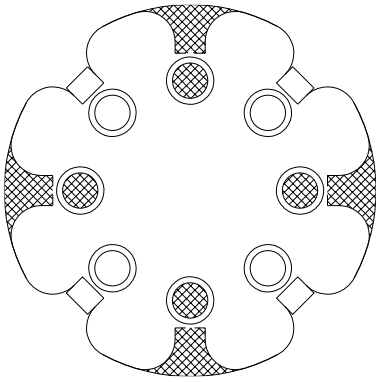
Another important function of the rod assembly is to establish the energy of the ions relative to the quadrupole. This is achieved through the application of the DC offset voltage on the rods. Due to collisional cooling through the skimmers and through the early portion of the octopole rods, the thermal energy of the ions has been all but eliminated. The flow transitions from transitional flow to molecular flow during the early portion of the octopole. As the ions experience their last molecular collision in this transition region, they are essentially

drifting downstream at the average gas velocity of the gas/ion stream entering the octopole from skimmer 2. Hence, the ions will have very uniform kinetic energies. Therefore, the field gradient between the octopole rods and the quadrupole rods, established by the DC offset on the rods and the zero volt DC offset on the quadrupole, sets the energy of the ions. The result is ions with uniform kinetic energy entering the quadrupole, resulting in uniform velocities for those ions with the same mass to charge ratio. The result from this uniformity is increased peak resolution. The DC offset on the octopole rods can be varied to alter the energy of the ions.

Design Notes:



The 8 rods are suspended in place by 4 chemically etched, Beryllium Copper rings. The purpose of the rings is to both suspend the rods as well as provide the electrical connection to the rods. The rods are soldered to tabs on the inside of the rings using Tin/Lead/Silver solder paste. Each set of rods are supported by two rings. As can be seen by careful examination of the diagram above, the rings for opposite rod polarities are separated by vespel spacers.



The graphic above depicts an end view of the rods supported by the rings. As can be seen, the rods are actually attached to fingers on the rings. In this case, the unhatched fingers are all part of the ring in the foreground whereas the hatched fingers are part of the ring in the background, 45 degrees offset. Since electrical contact is made through the rings, this is the method by which each set of rods is maintained at a common voltage and phase.

The entire assembly is housed in an aluminum tube. The tube provides protection for the octopole rods as well as provides a structure to mount the lens stack to. The tube has cutouts which are used to provide conductance to the Stage 3 vacuum system. These cutouts are important fpr proper operation and should not be changed without understanding of the affect on octopole performance. This can be somewhat difficult to determine since the actual pressure is not measured inside of the quadrupole.

Material Selection:

Both the rods and the rings are gold plated for two reasons. The first is to prevent oxidation of the components. Since the rods are made of carbide tool steel for high yield strength and the rings are made of Beryllium copper, both need a protective coating to prevent the metal from oxidizing and developing an insulation layer where charging effects could cause field disturbances. The second reason for the gold plating is to provide a good wetting surface for the solder.

The material choice for the rods was made in order to maintain straightness of the rods. Originally, stainless steel rods were used. Unfortunately, the rods were easily bent and the material would yield. It was nearly impossible to assemble a complete rod assembly without bending some of the rods. The stiffness and high yield strength of the tool steel provides the necessary straightness for the application. In addition, a tight straightness specification is placed on the drawing for the rods. The ferrous properties of the steel have not caused a problem in the ion optics since the RF signal essentially "demagnatizes" the rods continuously.

The material for the spacers, Vespel (polyimid), was chosen for its chemical inertness, low outgassing performance, and dimensional stability. In addition, the machinability made it an ideal candidate for the assembly. Since the ring positions reference off of the spacers, the rod spacing is ultimately determined by the

spacers. Rod positioning is critical to the operation of the octopole.

Assembly Capacitance:

Another important design characteristic of the rod assembly is the capacitance of the assembly. There are three important capacitances to be aware of:
- Between opposite polarity rods
- Between the rods and ground
- Between the last octopole ring and lens 2

The first two capacitances affect the RF drive circuitry for the RF voltage applied to the octopole rods. Since the rods have opposite polarity, adjacent rods form a capacitor. In addition, the entire rod assembly capacitance to ground also affects the circuitry. Therefore, changes to the mechanical configuration of the rods and/or rings cause changes in the capacitance which may affect the ability of the circuit to tune properly. Changes to the rods and/or rings in any way should be made cautiously with careful consideration of the effects on the circuitry.

The last capacitance mentioned, that between the last octopole ring and lens 2, is important because it couples the lens 2 voltage to the oscillating voltage applied to the rods. Since lens 2 is to be a static DC voltage, it has been decoupled by the use of bypass capacitance. Again, changes in the ring position should not be made with consideration of the affects to this portion of the circuit.

Manufacturing Concerns:

Much development was undertaken to improve the manufacturability of the rod assembly. The most difficult challenge was developing a soldering process which would provide a strong enough solder joint that could withstand both the assembly process and shock and vibration testing. Early prototypes suffered from weak joints which would often break just from the force required to remove the rod assembly from the fixture. Many experiments were performed to determine the correct solder alloy, solder amount, and melt temperature to develop a strong enough bond.

The final solder paste chosen (HP Part No 8090-1272) contains the following alloy - 62% Tin, 36% Lead, 2% Silver. Initially, it was thought that the solder joint strength could be improved by using an alloy with a higher silver content. In actuality, this resulted in a more brittle joint. The reason for this failure was thought to be an interaction with the gold plating which was being absorbed into the bond and causing the joint to be more brittle. As it turned out, the original solder, that which is being used now, was not being brought to a high enough temperature. By increasing the oven temperature from 200 C to 255 C, the bond strength improved dramatically without requiring a change in solder paste. Specifically, the GC oven is ramped from 50 to 255 C at a rate of 20 degrees per minute. Once at temperature, the oven holds for 2 minutes and then descends to 50 C at a rate of 30 degrees per minute. The slow ramp is necessary in order to evenly heat the assembly. This minimizes thermal distortion and keeps the rods as straight as possible. In fact, this is the reason for melting all of the solder simultaneously in an oven so that all of the joints are set at once which minimizes distortion due to differential heating.

One last note about solder - the solder amount specified in the assembly procedure was developed so that too much solder is not applied. If too much solder is applied, the solder will tend to wrap around the face of the rods. This can cause some disturbances in the electric field which will affect the ions. It is important to keep the faces of the rods as clear of defects as possible.

Areas for Improvement:

While the assembly has been greatly improved over the development of the octopole, it is still considered one of the more difficult assemblies to build. This is largely due to the application of the solder paste under the microscope. During the development, when the solder process was failing, an alternative brazed assembly was investigated. The furnace braze vendor did seem optimistic that a low temperature braze could be performed successfully. One of the main problems with this process, however, was that the braze temperature was close to the annealing temperature of the steel rods. Some early samples showed that the rods lost their strength and would yield rather easily. This process was never refined due to successful changes to the soldering process. The turnkey brazed assembly should be investigated as a possibility to reduce manufacturing cost. It should be noted, however, that there is considerable risk in this path as rod alignment may not be as controllable in the outsourced process.

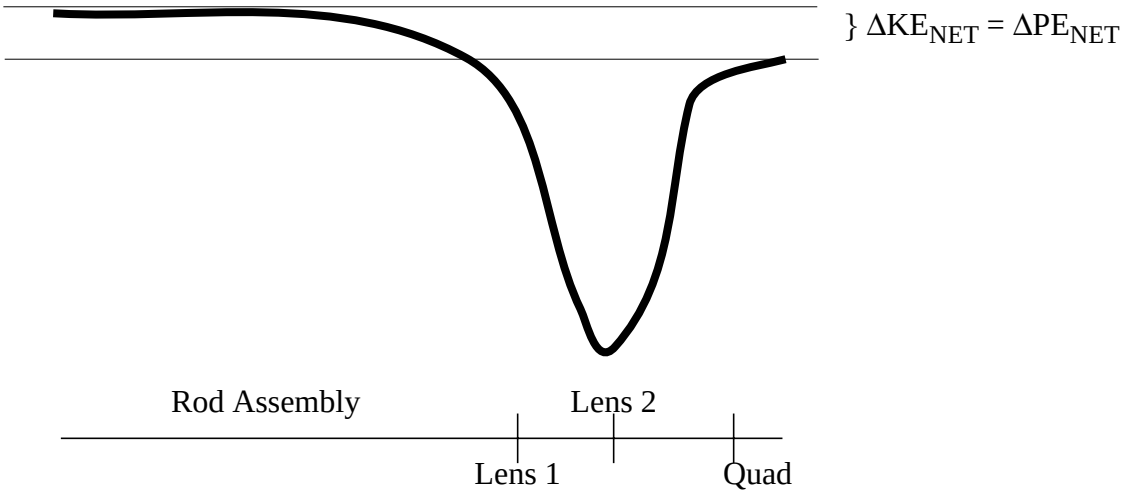
Lens Stack Assembly

The primary purposes of the lens stack are to focus the ions into the acceptance aperture of the quadrupole. In addition, the lenses shield the ions from the fringe fields at the ends of both the octopole and the quadrupole.

The voltage set on Lens 1, the first electrode that the ions will meet after leaving the octopole rods, is set a voltage slightly less than the DC offset on the rods. The purpose of lens 1 is to shield the ions from the fringe fields from the octopole rods. Directly behind it, Lens 2 has a much lower voltage. The field generated by these lenses helps to accelerate and draw the ions out of the octopole. It is important to note, however, that this acceleration does not add any net kinetic energy to the ions once they have been injected into the quadrupole since the ions must climb back up a potential energy "hill" to get to the ground state of the quadrupole rods. This is similar to a roller coaster rolling down a hill and then up a somewhat smaller hill. The ending kinetic energy is the same as if the original downhill stopped at the level of the top of the second hill.

Velocity/Energy Control

Below is a conceptual plot of potential energy (it should only be referenced for qualitative understanding of the energy states). The beginning of the plot indicates the kinetic energy of the ions after they have experienced their last molecular collision. This energy level is influenced by the average velocity of the gas during the early portion of the rods and any electrostatic effects from Skimmer 2. After that point, the energy state is controlled by electric fields. As the ions drift through the octopole rods, the kinetic energy changes very little since there are no collisions and the uniform DC offset on the rods does not establish an electric field in the axial direction. As the ions drift towards lens 1, which is typically held at a voltage of a few volts lower than the DC offset on the rods, the ions convert some potential energy into kinetic energy, thus accelerating. Lens 2 is set at a voltage much lower than the DC offset - actually the opposite sign. The large gradient greatly accelerates the ions and pulls them out of the rod assembly. However, as the ions leave, they must decelerate as they climb back up the potential energy curve to get to the much higher voltage of the quadrupole.



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Lens 2 also has the affect of injecting the ions into the quadrupole beyond the fringe fields at the ends of the quadrupole. This helps to improve the ion transmission and is the main reason why the lenses are tapered. The taper helps the lens reach into the quadrupole and has been deemed better than a snout like design which was used in the 59987A Electrospray Ion Source for MS Engine.

Another function of lens 2 is to provide the vacuum conductance limit between stages 3 and 4. Therefore, the orifice size and length of lens 2 are critical to limiting the gas load into stage 4. If the stage 4 pressure rises too high, the quadrupole mass analyzer will cease to function properly. There is actually no physical vacuum seal between stages 3 and 4. Instead, the OD of lens 2 fits into the ID of the ceramic ring on the front of the quadrupole. The tolerances on both of these dimensions are specified tight enough to provide sufficient restriction. Neither the nominal dimensions nor the tolerances should be changed without consideration to the effects on the vacuum system.

Design Notes:

Material Selection

The material for the lenses is 300 series stainless steel rather than nickel plated aluminum as was used for the skimmers. The reason for the use of stainless in this application is the need for dimensional stability and toughness. Furthermore, the parts do not pose as much of a machining challenge as did the skimmers.

The reason for the need for dimensional stability lies in the fact that the ion beam must be focused on an acceptance aperture of less than 0.1 mm in diameter. The positioning of the octopole assembly relative to the quadrupole is essential and is maintained by the OD of lens 2 and the ID of the ceramic ring on the front of the Mass Filter assembly. Since the Mass Filter is a heated zone, the temperature of lens 2 will change. Stainless steel will have less thermal expansion than aluminum and maintain alignment and fit much better.

In addition, it was feared that the abrasive ceramic on the lens would tend to remove the plating over time - either by removal or vibration. Therefore, the stainless steel provides the chemical inertness needed without any coatings.

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Theory of Operation

Introduction

A critical component of the LC/MSD system is the calibrant delivery system. The system, combined with the inlet control module, allows for the user to plumb in and deliver calibrant for both ES and APCI modes, all within the control of the data system. This means that the user does not need to prepare any samples nor replumb the instrument for tuning and operation modes. Furthermore, this system provides the capability of performing completely automated autotunes.

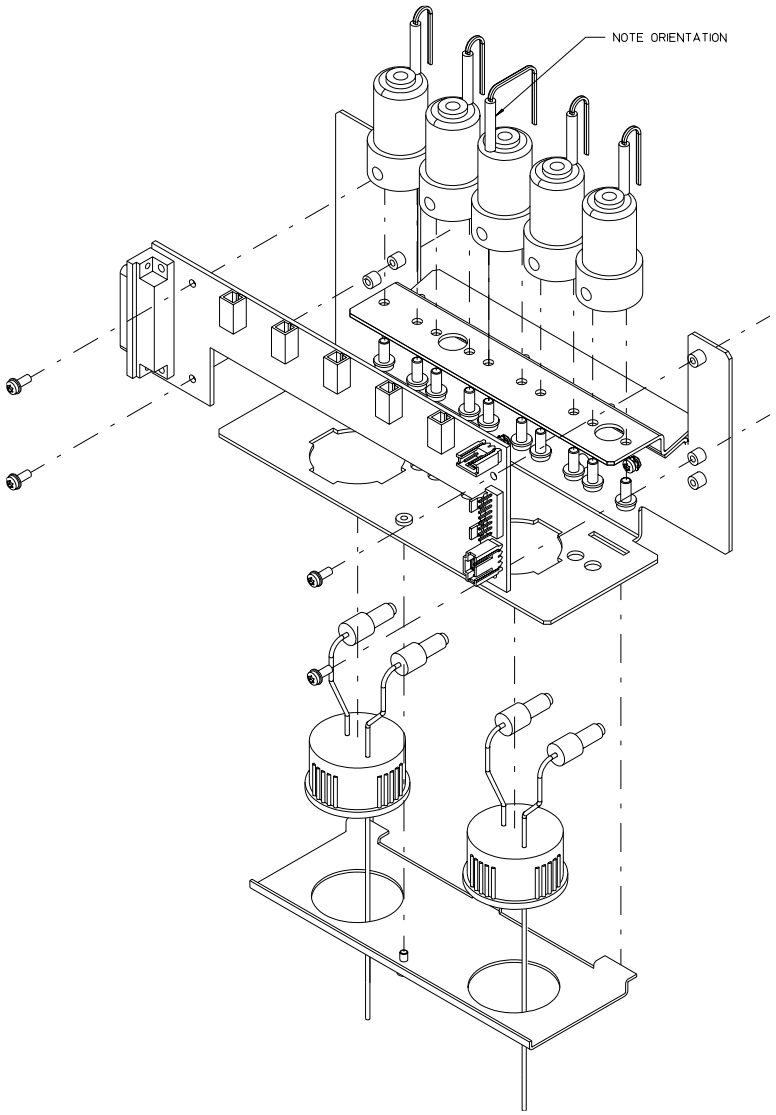
General Description

The CDS is capable of delivering two separate types of calibrant -- one for electrospray, the other for APCI. The liquid is delivered by the application of a positive head pressure above the fluid in gas tight bottles, thus forcing the fluid out through the delivery tube. The flow rate is controlled by the viscosity of the fluid, the diameter and length of the PEEK calibrant delivery tubing, the head pressure applied to the bottles, nebulizer needle diameter and length, as well as nebulizer exit conditions.

In electrospray mode, since the nebulizer needle is extended outside of the tip, the high speed gas reduces the pressure immediately outside the nebulizer exit. Since the local pressure is reduced below ambient, the calibrant can actually be siphoned out of the bottles if the shutoff valve is not closed. On the other hand, during APCI operation, the headspace pressure must exceed the positive back pressure induced by the recessed nebulizer needle. Since the APCI nebulizer needle is recessed, the flow slows down and increases the pressure immediately in front of the needle exit. Therefore, the headspace pressure must be large enough to counteract this force.

Five separate 3-way solenoid valves are used to distribute the gas and fluid both to and from the bottles, respectively. The valves, bottles, and control PCA are all mounted on one sheetmetal assembly which can be installed as an entire unit. In addition, integrated into the sheetmetal is a tray which contains a leak sensor, allowing for customer and data system notification of a calibrant or other fluid leak in the vicinity.

Hardware

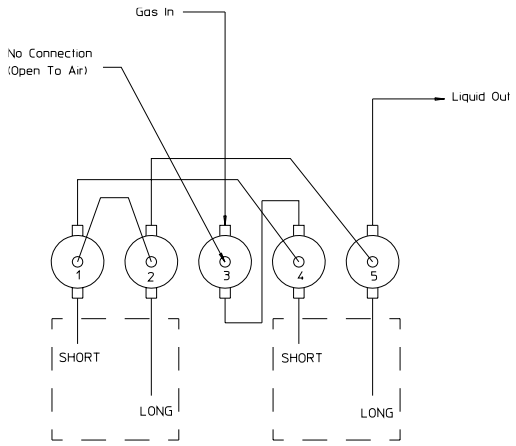


Valves:

The 5 valves chosen for this assembly are identical 24 volt 3-way solenoid valves produced by General Valve. Their bodies are constructed of Teflon while their valve seats and seals are made of Ethylene Propylene Diene Monomer (EPDM). Figure 1 shows how the valves are mounted while Figure 2 shows the schematic of the plumbing used to connect the valves.

The valves can be set to a number of different operating modes in order to deliver the correct calibrant to the liquid inlet selector valve.

As can be seen, valve 3 is oriented 180 degrees with respect to the other valves in the CDS Assembly. Valve 3 provides pressure relief when a leak is detected and when the calibrants are not in use.



PLUMBING SCHEMATIC
TOP VIEW

A contamination issue has been experienced with the CDS valves. The major source of contamination in the valves is due to ethylene propylene diene monomer (EPDM). Although this material is chemically resistant to acetonitrile/water (our tune mix solvents), it has a propensity to leach chemicals which are readily detected in API-ES and APCI modes.

Each valve contains two orings (one large, one small) and two valve seats. The valve seat EPDM material differs from the oring EPDM which further complicates matters (different chemical background). Extracting the orings and valve seats reduced the contamination significantly and left the parts otherwise unchanged. Below is a list of Electrospray contaminants contributed by the CDS.

Series 1 Ions (m/z)	**Series 2 Ions (m/z)**	**Series 3 Ions (m/z)**	**Series 4 Ions (m/z)**
289	333	391	435
303	347	405	449
317	361	419	463
331	375	433	477
345	389	447	491
359		461	505

Teflon encapsulated oring replacements were determined to be unsuitable due to their stiffness (potential seal failure) but did eliminate leaching.

Bottles:

Both CDS bottles are specially cleaned glass bottles which have been dipped in plastic to contain shattered bottles due to droppage or over-pressurization. The bottles are put through a special cleaning process to eliminate particulates. The caps contain a teflon liner for liquid and glass sealing.

In order to ensure that the bottle label faces forward in the calibrant tray on the left side of the instrument, the caps are installed into the assembly such that the threads align in the same orientation in all assemblies. The labels are also installed on the bottles such that the text is aligned to the threads. The combination of these processes ensures that the labelling will face outward.

The caps are also modified so that the pneumatic and fluid tubing can be fed through the cap. Slightly undersized holes are drilled through both the cap and liner such that the tubing seals against the plastic when inserted.

Tubing:

All of the gas and liquid tubing within the CDS is Tefzel to provide chemical compatibility with solvents and calibrants. The downstream PEEK delivery tubing restriction is preverified within a specific flow range to ensure proper downstream restriction.

Fittings:

All of the fittings used are either Tefzel or PEEK with a PEEK ferrule. The Tefzel fittings are used on all of the permanent fittings while the PEEK fittings are used on the user-accessible fittings.

Bubble Problems:

During the CDS development, a problem associated with calibrant peak instability was identified. The cause was attributed to gas bubbles trapped in the dead volume of the CDS valves and downstream plumbing. Their presence lead to intermitent flow interruptions which resulted in peak dropouts. Resolution of the problem has been implemented in firmware by providing additional gas purge time to clear liquid calibrant from the lines following the calibrant shutoff.

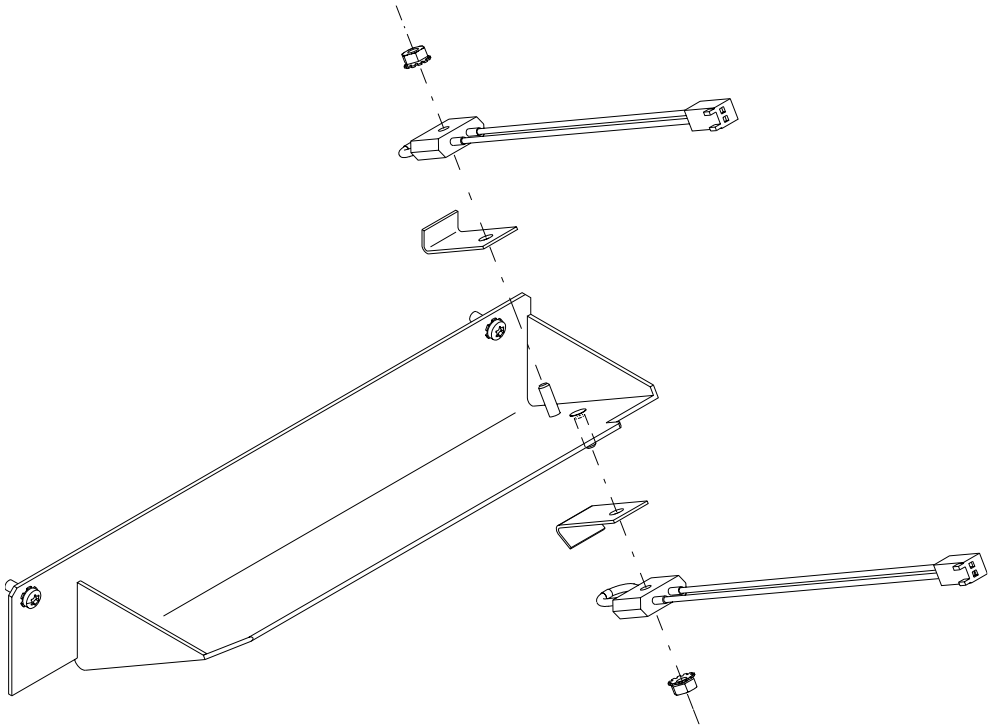
Leak Sensor:

Two leak sensors are actually included in the leak sensing tray. The top leak sensor, shown in the graphic below, is the sensor which comes in contact with the liquid, while the bottom leak sensor is used as a reference. The leak sensors are actually thermistors which are kept in the same thermal environment.

A regulated current flows through each thermistor causing voltage drop differences based on temperature differences of the thermistors. As liquid comes in contact with the top thermistor, the voltage drop changes relative to the lower thermistor, thus triggering a flag to the data system.

It is extremely important that the thermistor sensors be kept in the same ambient thermal environment such that the sensors are not activated due to local changes in the thermal environment, resulting in false triggers. Therefore, the thermistors are kept in close contact to the same portion of the tray so that they experience similar thermal fluctuations.

Should a leak be detected at the CDS, the firmware will return the CDS to standby state and vent the CDS bottles so as to stop the flow of calibrant. This will prevent the leak from emptying the entire bottle of calibrant.



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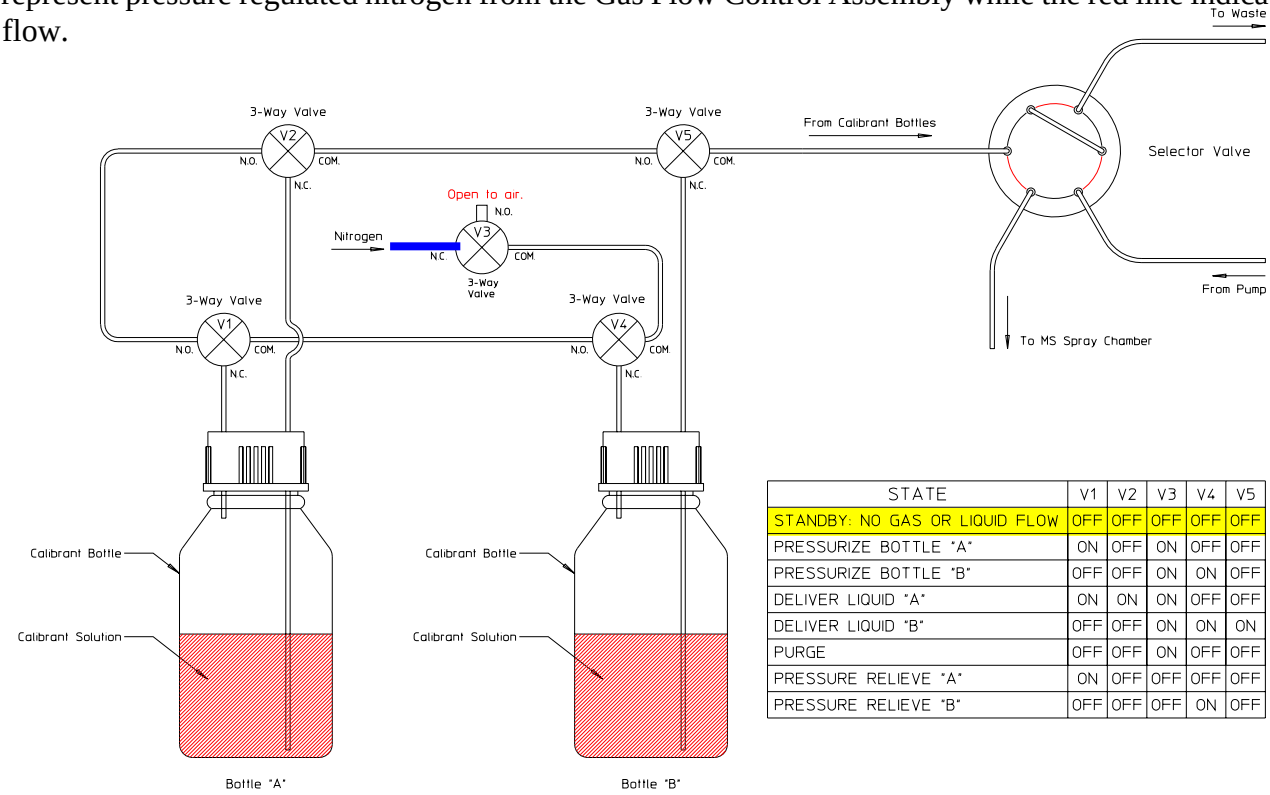
Operating Modes:

There are several different firmware controlled operating modes of the calibrant delivery system. Below the following list of the modes, is a graphic depicting the valve states for each of the modes.

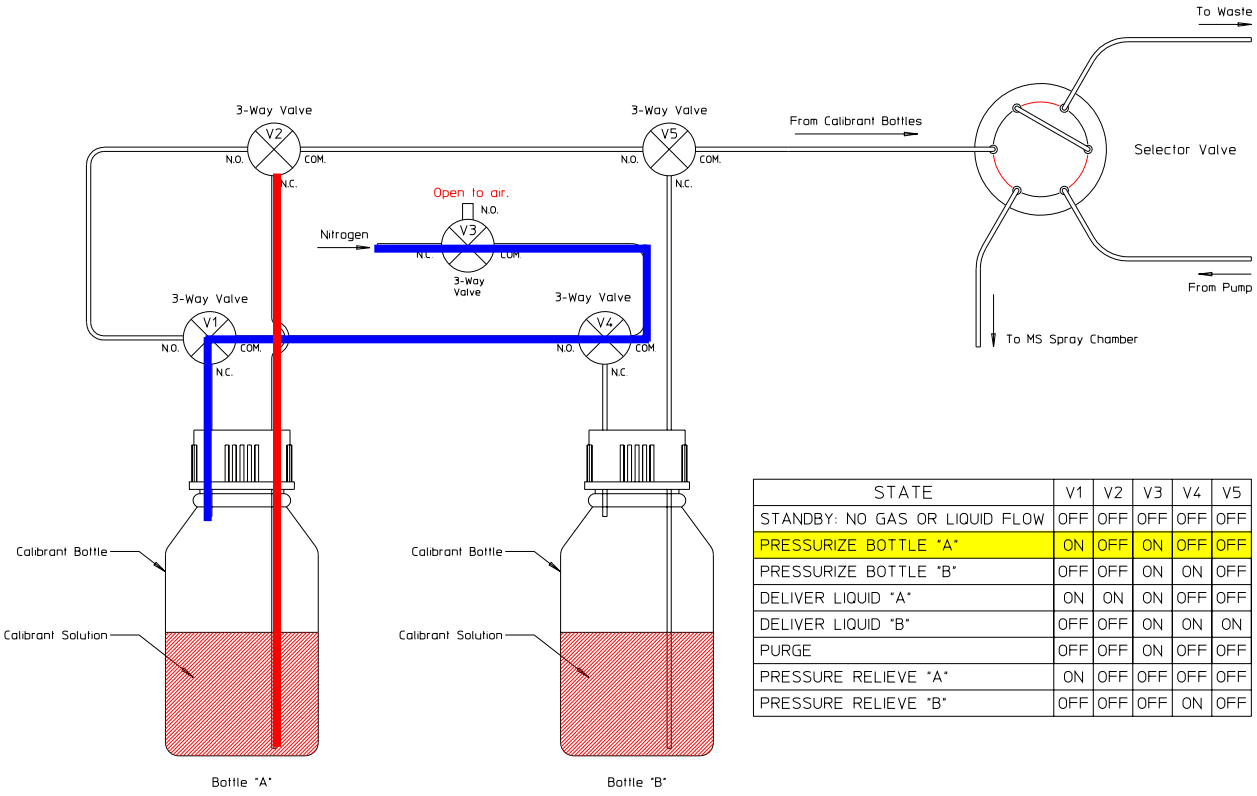
State	Description
Standby	All valves closed - no gas or liquid flow
Pressurize A	Pressurizes A bottle head space
Pressurize B	Pressurizes B bottle head space
Deliver A	Pressurizes A bottle and releases liquid A flow
Deliver B	Pressurizes B bottle and releases liquid B flow
Purge	Allows gas to flow through main line
Relieve A	Vents bottle A to atmosphere
Relieve B	Vents bottle B to atmosphere

Valve State Diagrams

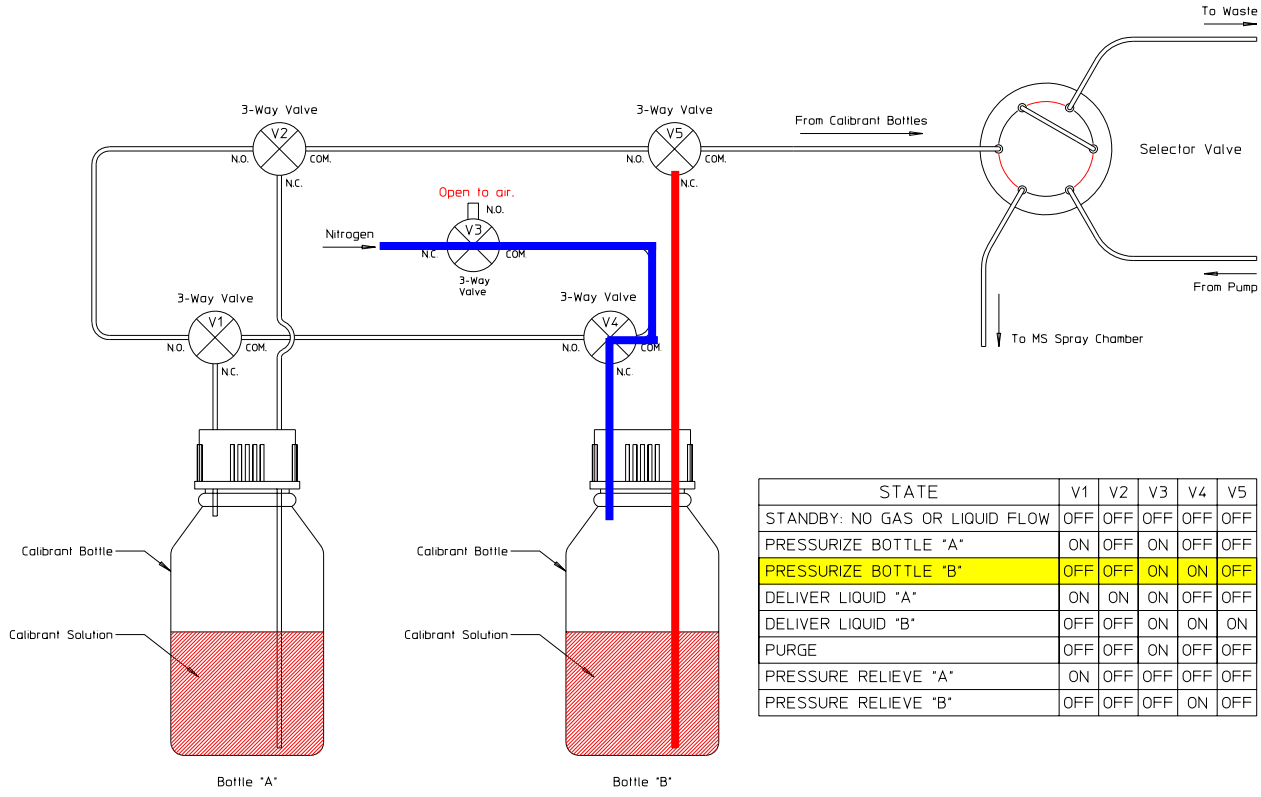
The following diagrams show the gas and liquid flow through the CDS in each of the operating states. Blue lines represent pressure regulated nitrogen from the Gas Flow Control Assembly while the red line indicates the fluid flow.



STATE	V1	V2	V3	V4	V5
STANDBY: NO GAS OR LIQUID FLOW	OFF	OFF	OFF	OFF	OFF
PRESSURIZE BOTTLE "A"	ON	OFF	ON	OFF	OFF
PRESSURIZE BOTTLE "B"	OFF	OFF	ON	ON	OFF
DELIVER LIQUID "A"	ON	ON	ON	OFF	OFF
DELIVER LIQUID "B"	OFF	OFF	ON	ON	ON
PURGE	OFF	OFF	ON	OFF	OFF
PRESSURE RELIEVE "A"	ON	OFF	OFF	OFF	OFF
PRESSURE RELIEVE "B"	OFF	OFF	OFF	ON	OFF



STATE	V1	V2	V3	V4	V5
STANDBY: NO GAS OR LIQUID FLOW	OFF	OFF	OFF	OFF	OFF
PRESSURIZE BOTTLE "A"	ON	OFF	ON	OFF	OFF
PRESSURIZE BOTTLE "B"	OFF	OFF	ON	ON	OFF
DELIVER LIQUID "A"	ON	ON	ON	OFF	OFF
DELIVER LIQUID "B"	OFF	OFF	ON	ON	ON
PURGE	OFF	OFF	ON	OFF	OFF
PRESSURE RELIEVE "A"	ON	OFF	OFF	OFF	OFF
PRESSURE RELIEVE "B"	OFF	OFF	OFF	ON	OFF



STATE	V1	V2	V3	V4	V5
STANDBY: NO GAS OR LIQUID FLOW	OFF	OFF	OFF	OFF	OFF
PRESSURIZE BOTTLE "A"	ON	OFF	ON	OFF	OFF
PRESSURIZE BOTTLE "B"	OFF	OFF	ON	ON	OFF
DELIVER LIQUID "A"	ON	ON	ON	OFF	OFF
DELIVER LIQUID "B"	OFF	OFF	ON	ON	ON
PURGE	OFF	OFF	ON	OFF	OFF
PRESSURE RELIEVE "A"	ON	OFF	OFF	OFF	OFF
PRESSURE RELIEVE "B"	OFF	OFF	OFF	ON	OFF

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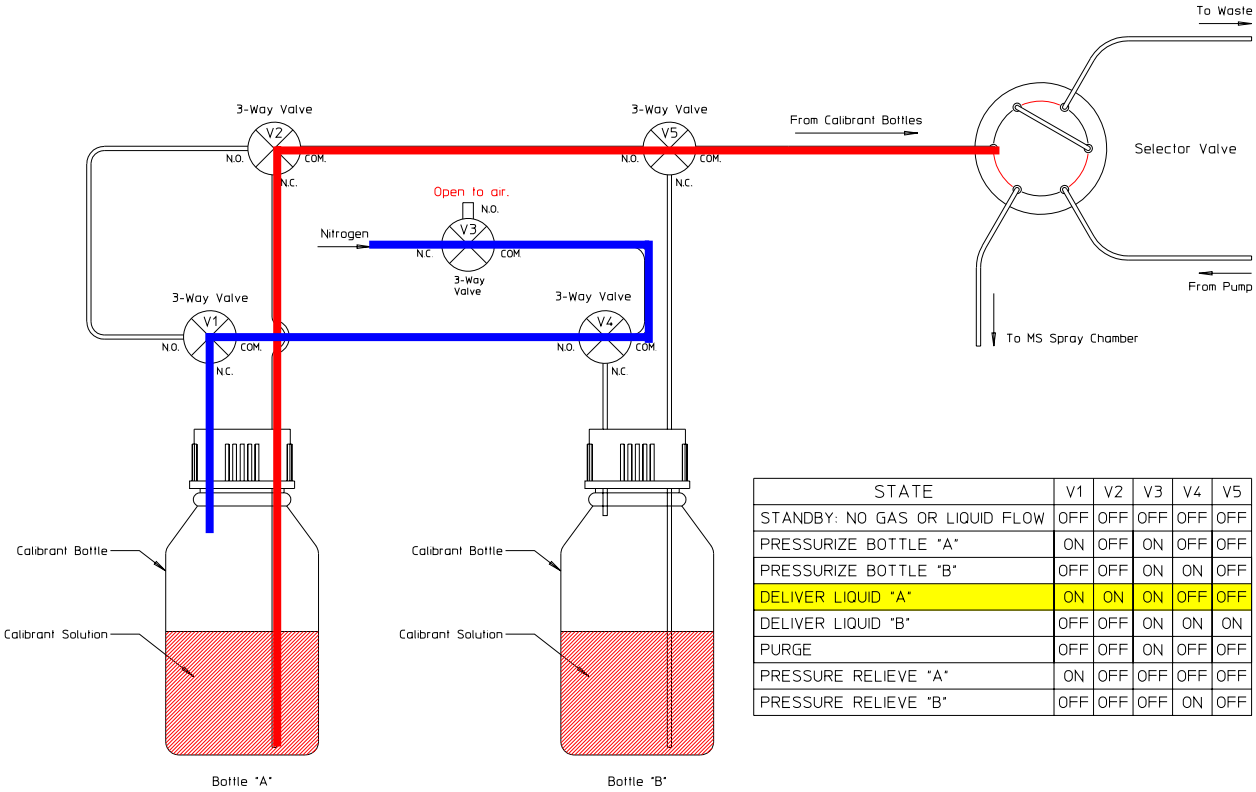
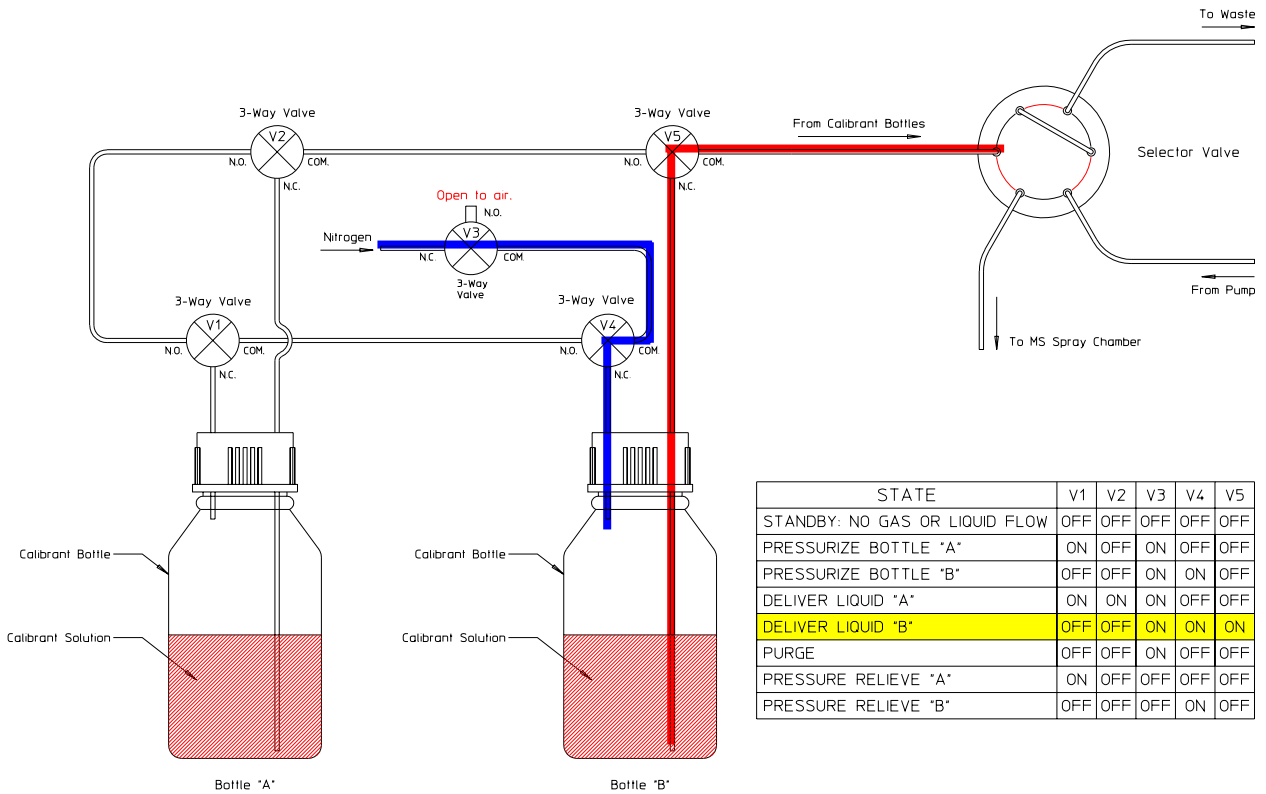


STATE	V1	V2	V3	V4	V5
STANDBY: NO GAS OR LIQUID FLOW	OFF	OFF	OFF	OFF	OFF
PRESSURIZE BOTTLE "A"	ON	OFF	ON	OFF	OFF
PRESSURIZE BOTTLE "B"	OFF	OFF	ON	ON	OFF
DELIVER LIQUID "A"	ON	ON	ON	OFF	OFF
DELIVER LIQUID "B"	OFF	OFF	ON	ON	ON
PURGE	OFF	OFF	ON	OFF	OFF
PRESSURE RELIEVE "A"	ON	OFF	OFF	OFF	OFF
PRESSURE RELIEVE "B"	OFF	OFF	OFF	ON	OFF



STATE	V1	V2	V3	V4	V5
STANDBY: NO GAS OR LIQUID FLOW	OFF	OFF	OFF	OFF	OFF
PRESSURIZE BOTTLE "A"	ON	OFF	ON	OFF	OFF
PRESSURIZE BOTTLE "B"	OFF	OFF	ON	ON	OFF
DELIVER LIQUID "A"	ON	ON	ON	OFF	OFF
DELIVER LIQUID "B"	OFF	OFF	ON	ON	ON
PURGE	OFF	OFF	ON	OFF	OFF
PRESSURE RELIEVE "A"	ON	OFF	OFF	OFF	OFF
PRESSURE RELIEVE "B"	OFF	OFF	OFF	ON	OFF

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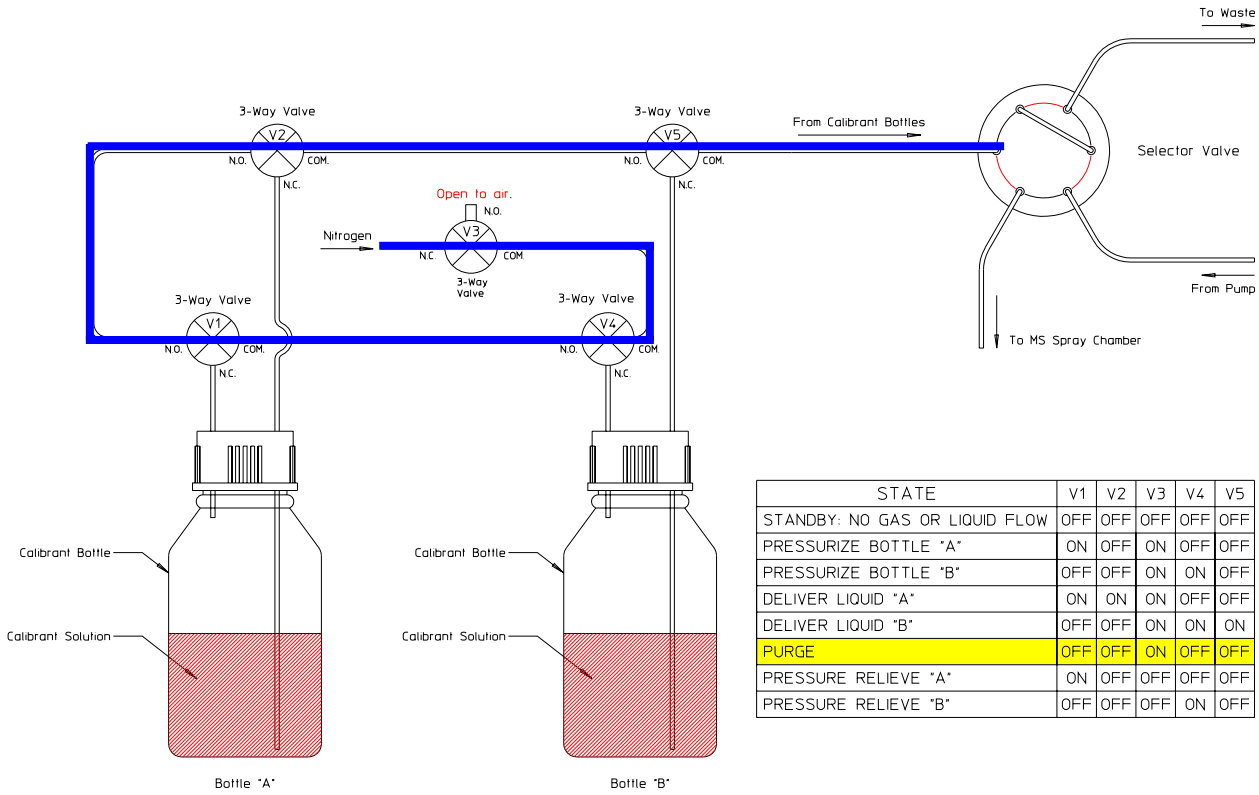

STATE	V1	V2	V3	V4	V5
STANDBY: NO GAS OR LIQUID FLOW	OFF	OFF	OFF	OFF	OFF
PRESSURIZE BOTTLE "A"	ON	OFF	ON	OFF	OFF
PRESSURIZE BOTTLE "B"	OFF	OFF	ON	ON	OFF
DELIVER LIQUID "A"	ON	ON	ON	OFF	OFF
DELIVER LIQUID "B"	OFF	OFF	ON	ON	ON
PURGE	OFF	OFF	ON	OFF	OFF
PRESSURE RELIEVE "A"	ON	OFF	OFF	OFF	OFF
PRESSURE RELIEVE "B"	OFF	OFF	OFF	ON	OFF

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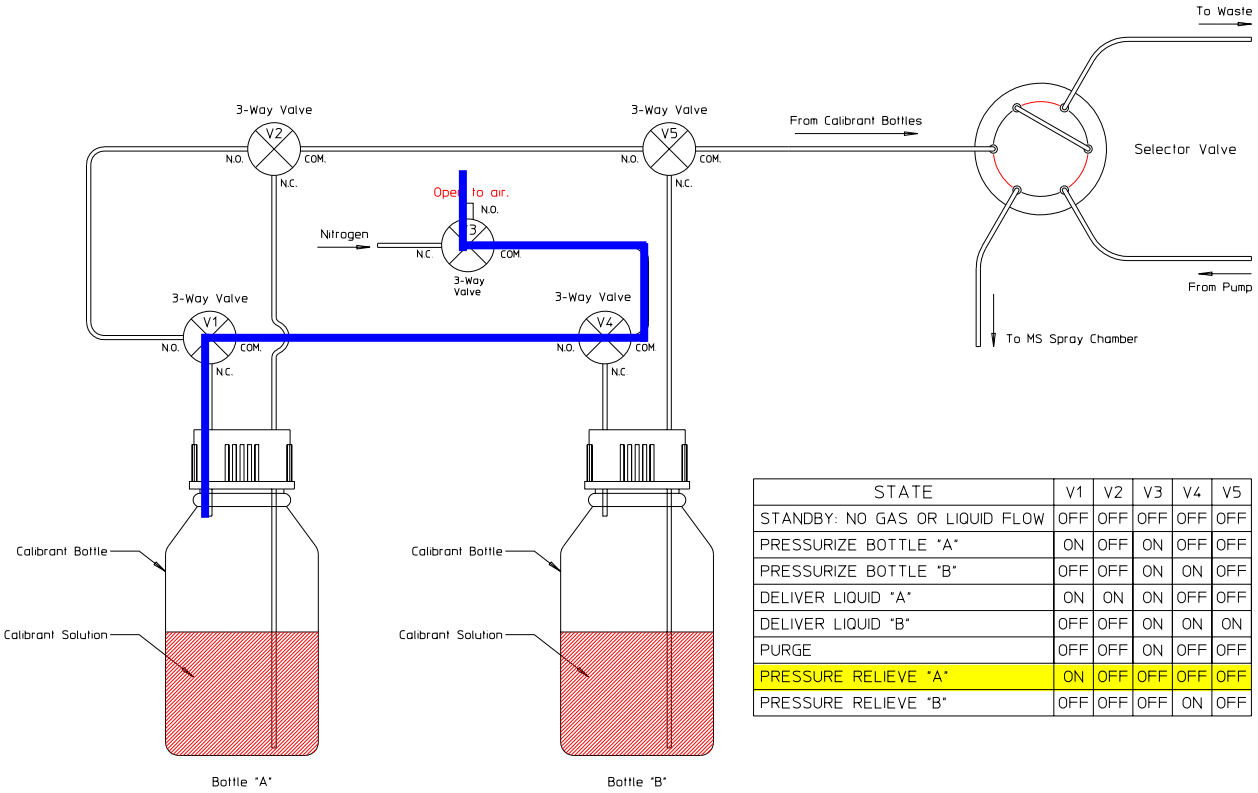
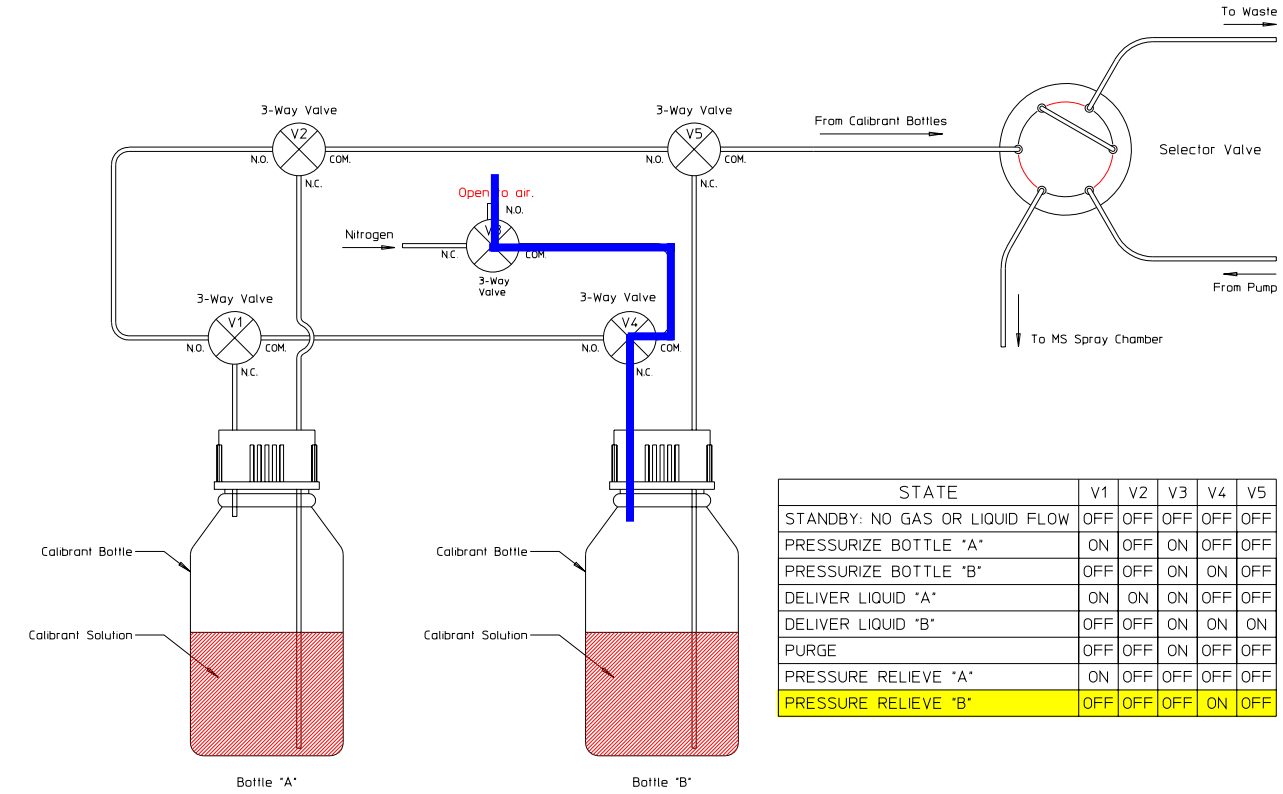


STATE	V1	V2	V3	V4	V5
STANDBY: NO GAS OR LIQUID FLOW	OFF	OFF	OFF	OFF	OFF
PRESSURIZE BOTTLE "A"	ON	OFF	ON	OFF	OFF
PRESSURIZE BOTTLE "B"	OFF	OFF	ON	ON	OFF
DELIVER LIQUID "A"	ON	ON	ON	OFF	OFF
DELIVER LIQUID "B"	OFF	OFF	ON	ON	ON
PURGE	OFF	OFF	ON	OFF	OFF
PRESSURE RELIEVE "A"	ON	OFF	OFF	OFF	OFF
PRESSURE RELIEVE "B"	OFF	OFF	OFF	ON	OFF



STATE	V1	V2	V3	V4	V5
STANDBY: NO GAS OR LIQUID FLOW	OFF	OFF	OFF	OFF	OFF
PRESSURIZE BOTTLE "A"	ON	OFF	ON	OFF	OFF
PRESSURIZE BOTTLE "B"	OFF	OFF	ON	ON	OFF
DELIVER LIQUID "A"	ON	ON	ON	OFF	OFF
DELIVER LIQUID "B"	OFF	OFF	ON	ON	ON
PURGE	OFF	OFF	ON	OFF	OFF
PRESSURE RELIEVE "A"	ON	OFF	OFF	OFF	OFF
PRESSURE RELIEVE "B"	OFF	OFF	OFF	ON	OFF

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A	AS ISSUED PER PC23-6030	N. Moreyra	10/13/97

E. Aisawa DRAWN BY	10/13/97	**Sprite Pirani Gauge** **ERS** TITLE	HEWLETT PACKARD
E. Aisawa ENGINEER	10/13/97		
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1.0 Pirani Gauge Interface

The purpose of this document is to set forth the electrical and communication specifications for the pirani gauge module that will be used in the Sprite instrument (G1946A). Since the pirani gauge module has been designated as a non-real time subsystem module, the specifications for the communication interface will be governed by the Non-Real Time Subsystem (NRTS) ERS specification (A-G1946-90017-1). The network variables for the Pirani Gauge will be defined in this specification.

1.1 Temperature and Humidity

The gauge module will be tested to Hewlett-Packard's standard tests for a Class B2 instrument with the following exceptions:

1.1.1 Minimum ambient operating temperature: 15 deg C (tested to 10 deg C)

1.1.2 Maximum ambient operating temperature: 35 deg C (tested to 40 deg C)

1.2 EMC requirements

The pirani gauge module will comply with all of the standards that the Sprite instrument will be held accountable for. The intent here is that the design team will not have to do anything special with the gauge module in order for the instrument to pass its tests.

1.3 Physical Connection

The gauge module will attach to the vacuum manifold via a NW16KF Stainless Steel flange.

1.4 Mains Power

The gauge module will derive all of its power from the Network connector and will necessarily be restricted by this fact.

1.5 Network Power

1.5.1 Current draw from the +24V DC lines on the network connector shall be less than 1 amp.

1.5.2 There should be sufficient isolation within the gauge module such that a failure within the module does not drag down the +24V supply lines.

1.6 Communication Connector

The controller will use a shielded 8 position, 8 contact RJ45 connector as shown in Figure 1.

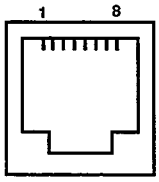


Figure 1: Pirani Gauge Network Connector

1.6.1 Pin Definitions

1.6.1.1 Pin 1: +EIA485

1.6.1.2 Pin 2: -EIA485

1.6.1.3 Pin 3: Power Ground

1.6.1.4 Pin 4: +24 Volts

1.6.1.5 Pin 5: +24 Volts

1.6.1.6 Pin 6: Power Ground

1.6.1.7 Pin 7: Signal Ground

1.6.1.8 Pin 8: Reserved by Echelon Corporation

1.7 Bus Termination

The pirani gauge should not have any internal terminations on the signal lines.

1.8 Installation

Refer to the NRTS ERS section, *Installation of subsystem elements.*

1.9 Network Variable Inputs

1.9.1 *Mode [CI_mode]* - Enumerated type which tells a node whether to operate normally, perform a self test, or go into a diagnostic mode. Not all options need be implemented to use this variable.

1.9.2 *Event Selector [EI_event_select]* - A network variable that selects an event from the event log(s) (0 is the most recent event).

1.9.3 *System Date-Time [EI_sysdate]* - Sets the system date and time. This variable should be updated periodically (typically once a second).

1.9.4 *CI_filerequest [NVI_filerequest]* - Specifies to the device which file should be uploaded to the host.

1.9.5 *Part Number Information [NI]*

1.9.6 *Select Factory Defaults [CI_defaults]* - Restores the span calibration, the zero calibration, and the gasnumber to their factory set values.

1.9.7 *Gas Calibration Curve Selector [CI_gasnumber]* - Selects the gas curve the gauge is calibrated for.

1.9.8 *Flush Internal Timers [MI_flush_countrs]* - Immediately updates non-volatile timer memory.

1.9.9 *Reset Internal Timers [MI_reset_timers]* - Allows the module's internal timers to be reset.

1.9.10 *MI_span* - Variable for calibration

1.9.11 *MI_zero* - Variable for calibration

1.9.12 *MI_factory_span* - Variable for factory calibration

1.9.13 *MI_factory_zero* - Variable for factory calibration

1.9.14 *wink* - Network management message. Node responds by flashing service pin indicator.

1.9.15 *Pressure Change Threshold [SPV_threshold]* - The percentage change in pressure above which would cause the module to override the update period and cause the pressure reading to be output immediately. This setpoint would be stored in non-volatile memory.

1.9.16 *Control Configuration [CC]*

The following structure field definitions are used by the manufacturer and the system integrator to stagger starting and stopping transients and network traffic in the situation where multiple pumps are present. This information is accessible to anyone, is written into the node by the element's manufacturer and/or integrator, and is stored in non-volatile memory.

1.9.16.1 *Pressure Reporting Update Period [SPV_update_period]* - The amount of time allowed before a pressure reading is output. A change in pressure exceeding the threshold will be reported immediately, regardless of the status of the update period. This setpoint will be stored in non-volatile memory.

1.9.16.2 *Pressure Reporting Update Delay [SPV_update_delay]* - The amount of time after the expiration of the update period before a pressure reading is output. The purpose of this setpoint is to stagger pressure output readings from multiple gauges to avoid potential collisions. This setpoint will be stored in non-volatile memory.

1.10 Network Variable Outputs

1.10.1 *Status Information [SO]*

The following structure field definitions are used to communicate the status of a Pirani gauge.

1.10.1.1 *On-Off Status [on]* - This field communicates the ON-OFF state of the gauge.

1.10.1.2 *Warning Information [warn]* - This field is defined by the gauge manufacturer. The restriction here is that there are only 16 different warning conditions that can be reported in this variable.

1.10.1.3 *Shutdown Information [shutdown]* - This field has the same restriction as the Warning field.

1.10.2 *Pressure readout [SO_pressure]* - This variable reports the pressure reading.

1.10.3 *Selected Gas Calibration Curve [SO_gas]* - This variable reports the gas that the gauge is calibrated for.

1.10.4 *Service Output [MO]*

The following structure field definitions are used to extract maintenance information from the gauge. This information is stored in non-volatile memory.

1.10.4.1 *Total Time [total_time]* - This variable reports the total time that the gauge has been on.

1.10.4.2 *Process Time [total_proc]* - This field reports the total time that the gauge has been in its ON state.

1.10.4.3 *Service Time [serv_time]* - This field reports the approximate total ON time of the gauge to the next service.

1.10.4.4 *Process Service Time [serv_proc]* - This field reports the approximate process time of the gauge to the next service.

1.10.4.5 *Number of ON/OFF Cycles [cycles]* - This field reports the number of ON/OFF cycles that the gauge has undergone.

1.10.4.6 *Cycle Service Time [serv_cycles]* - This field reports the approximate number of ON/OFF cycles that the gauge has before the next service.

1.10.5 *Event Log Output Information [EO]*

The following structure field definitions are used to communicate a requested event log entry (if event logs are implemented on the node).

1.10.5.1 *Event Entry Retrieval from the On-Off Event Log [on_off_event]* - This field shows the on-off state from the requested event entry.

1.10.5.2 *Event Entry Retrieval from the Warning Event Log [warn_event]* - This field shows the Warning Status state from the requested event entry.

1.10.5.3 *Event Entry Retrieval from the Shutdown Event Log [shutdown_event]* - This field shows the Shutdown Status state from the requested event entry.

1.10.5.4 *System Date and Time Entry from Event Log [mark_event]* - This field shows the time that the requested event entry was logged.

1.10.6 *NVO_filestatus* - The device uses this network variable to inform the host of the status of the file transfer.

1.10.7 *Identification [NO]*

The following structure field definitions are used to identify the revision level and manufacturer of the subsystem hooking up to the Non-Real Time bus. This information is accessible to anyone, is written into the node by the element's manufacturer, and is stored in non-volatile memory. These identification constants are directly readable as ASCII strings by polling the element.

1.10.8 *Hardware Identification [NH]*

1.10.9 *Subsystem Element Calibration conditions [NO_conditions]* - An optional network variable structure containing the following fields:

1.10.10 *Subsystem Element Configuration [NVO_mfrconfig]* - A manufacturer-optional designation which further defines the subsystem element's configuration. Expressed as a 30-character ASCII string.

1.11 Neuron® C Data Structures and Definitions

This section will repeat information found in the NRTS ERS document in order to have all the variable definitions for the Pirani gauge in one place.

Command		Refer to Section
typedef enum {		
normal	=0;	
self_test	=1;	
ext_test	=2;	
diagnostic	=3;	
} control_mode;		NRTS ERS
network input control_mode CI_mode = normal;		NRTS ERS
network input		
sd_string (“Selects the event output on event out variables.”)		
SNVT_count EI_event_select;		NRTS ERS
network input		
sd_string (“System Date and Time information”)		
SNVT_time_stamp EI_sysdate;		NRTS ERS
network input SNVT_file_req NVI_filerequest		NRTS ERS
typedef struct {		
char_10	hw_sn;	NRTS ERS
char_10	oem_part;	NRTS ERS
char_10	user_tag;	NRTS ERS
} part_number;		
network input eeprom part_number NI;		NRTS ERS

network input

sd_string (“Returns MI_span, MI_zero, and CI_gasnumber to their factory preset values.”)

config SNVT_lev_disc CI_defaults; 1.9.6

network input

sd_string (“Selects the gas the gauge output is calibrated for. Gas numbers should be defined here.”)

config SNVT_count CI_gasnumber = 0; 1.9.7

network input

SNVT_lev_disc MI_flush_countrs

network input

sd_string (“ST_ON resets all internal counters and timers”)

SNVT_lev_disc MI_reset_timers = ST_OFF; 1.9.9

network input

SNVT_press_f MI_span; 1.9.10

network input

SNVT_press_f MI_zero; 1.9.11

network input

SNVT_press_f MI_factory_span; 1.9.12

network input

SNVT_press_f MI_factory_zero; 1.9.13

wink 1.9.14

network input

sd_string (“Set Point Value for the percentage change in pressure allowed above which the pressure will be reported immediately.”)

config SNVT_lev_count SPV_threshold = 2; 1.9.15

```
typedef struct {
        SNVT_time_passed    update_period;          1.9.16.1
        SNVT_time_passed    update_delay;           1.9.16.2
} control_config_t;

network input
   config control_config CC = {0,0,2,0, 0,0,0,100};          1.9.16
```

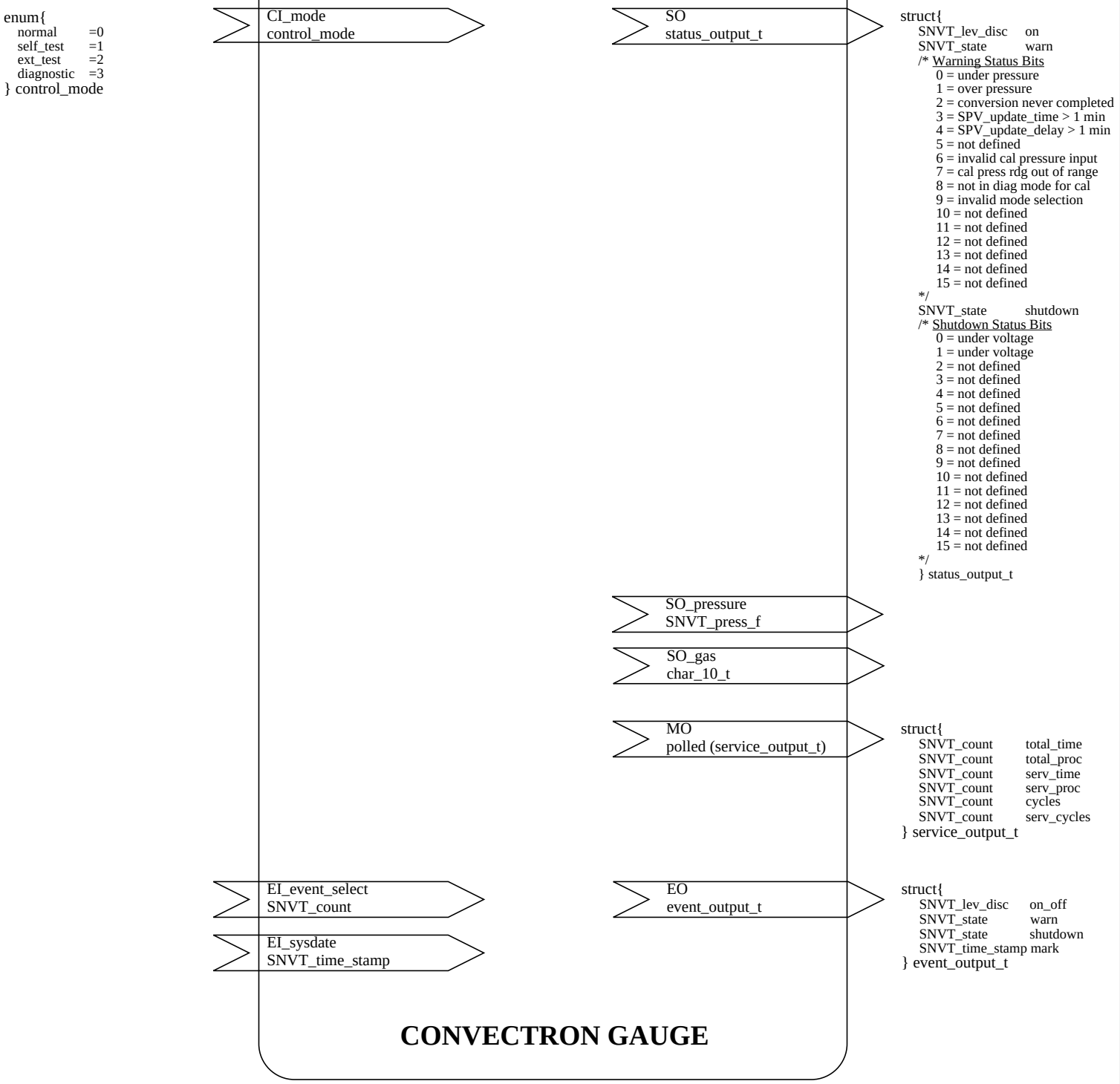
```
typedef struct {
    SNVT_lev_disc       on;                 NRTS ERS
    SNVT_state          warn;               NRTS ERS
    /* Warning Status Bits
        0 = under pressure
        1 = over pressure
        2 = conversion never completed
        3 = SPV_update_time > 1 min
        4 = SPV_update_delay > 1 min
        5 = not defined
        6 = invalid cal pressure input
        7 = cal press rdg out of range
        8 = not in diag mode for cal
        9 = invalid mode selection
        10 = not defined
        11 = not defined
        12 = not defined
        13 = not defined
        14 = not defined
        15 = not defined
    */
    SNVT_state          shutdown;           NRTS ERS
    /* Shutdown Status Bits
        0 = under voltage
        1 = over voltage
        2 = motor temp
        3 = not defined
        4 = not defined
        5 = not defined
        6 = not defined
        7 = not defined
        8 = not defined
        9 = not defined
        10 = not defined
        11 = not defined
        12 = not defined
        13 = not defined
        14 = not defined
        15 = not defined
    */
} status_output;
```

E. Aisawa DRAWN BY	10/13/97	**Sprite Pirani Gauge ERS** TITLE	HEWLETT PACKARD
E. Aisawa ENGINEER	10/13/97		
N. Moreyra RELEASE TO PROD.	10/13/97		G1946-80004 PART NUMBER
SUPERSEDES DWG.	CURRENT REV A	PAGE 9 OF 13	**A-G1946-80004-8**

```
network output
  sd_string ("Pressure reading from gauge in Pascals.")
  SNVT_press_f SO_pressure;                                   1.10.2

typedef struct {
      char                ascii[10];
} char_10;

network output
  sd_string ("Name of Gas that the gauge output is calibrated for.")
  char_10 SO_gas;                                             1.10.3

typedef struct {
      SNVT_count          total_time;                         1.10.4.1
      SNVT_count          total_proc;                         1.10.4.2
      SNVT_count          serv_time;                          1.10.4.3
      SNVT_count          serv_proc;                          1.10.4.4
      SNVT_count          cycles;                             1.10.4.5
      SNVT_count          serv_cycles;                        1.10.4.6
} service_output_t;

network output polled service_output_t MO;                    1.10.4

typedef struct {
      SNVT_lev_disc       on_off;                             NRTS ERS
      SNVT_state          warn;                               NRTS ERS
      SNVT_state          shutdown;                           NRTS ERS
      SNVT_time_stamp     mark;                               NRTS ERS
} event_output_t;

network output event_output_t EO;                             NRTS ERS

network output SNVT_file_status NVO_filestatus                NRTS ERS
```

```
typedef struct {
        char_10                 hw_code_no;                     NRTS ERS
        char_10                 sw_code_no;                     NRTS ERS
        char_10                 manufacturer;                   NRTS ERS
} rev_levels_t;

network output
  const rev_levels_t NO =       {
                                “011411-102”,                   NRTS ERS
                                “PP11520109”,                   NRTS ERS
                                “       GP”                     NRTS ERS
                                };

typedef struct {
        char_10                 hw_sn;                          NRTS ERS
        char_10                 oem_part;                       NRTS ERS
        char_10                 users_tag;                      NRTS ERS
} part_number_t;

network output const part_number_t NH =                         NRTS ERS
                                {
                                “ForelineGg”,                   NRTS ERS
                                "       OEM”,                   NRTS ERS
                                “Tag1.00.00”                    NRTS ERS
                                };

typedef struct {
        SNVT_time_stamp         caldate;                        NRTS ERS
        char_10_t               comment;                        NRTS ERS
} cal_conditions_t;

network output eeprom cal_conditions_t NO_conditions            NRTS ERS

network output eeprom SNVT_str_asc NVO_mfrconfig                NRTS ERS
```

EXTERNAL INTERFACE SECTION



E. Aisawa DRAWN BY	10/13/97	**Sprite Pirani Gauge ERS** TITLE	HEWLETT PACKARD
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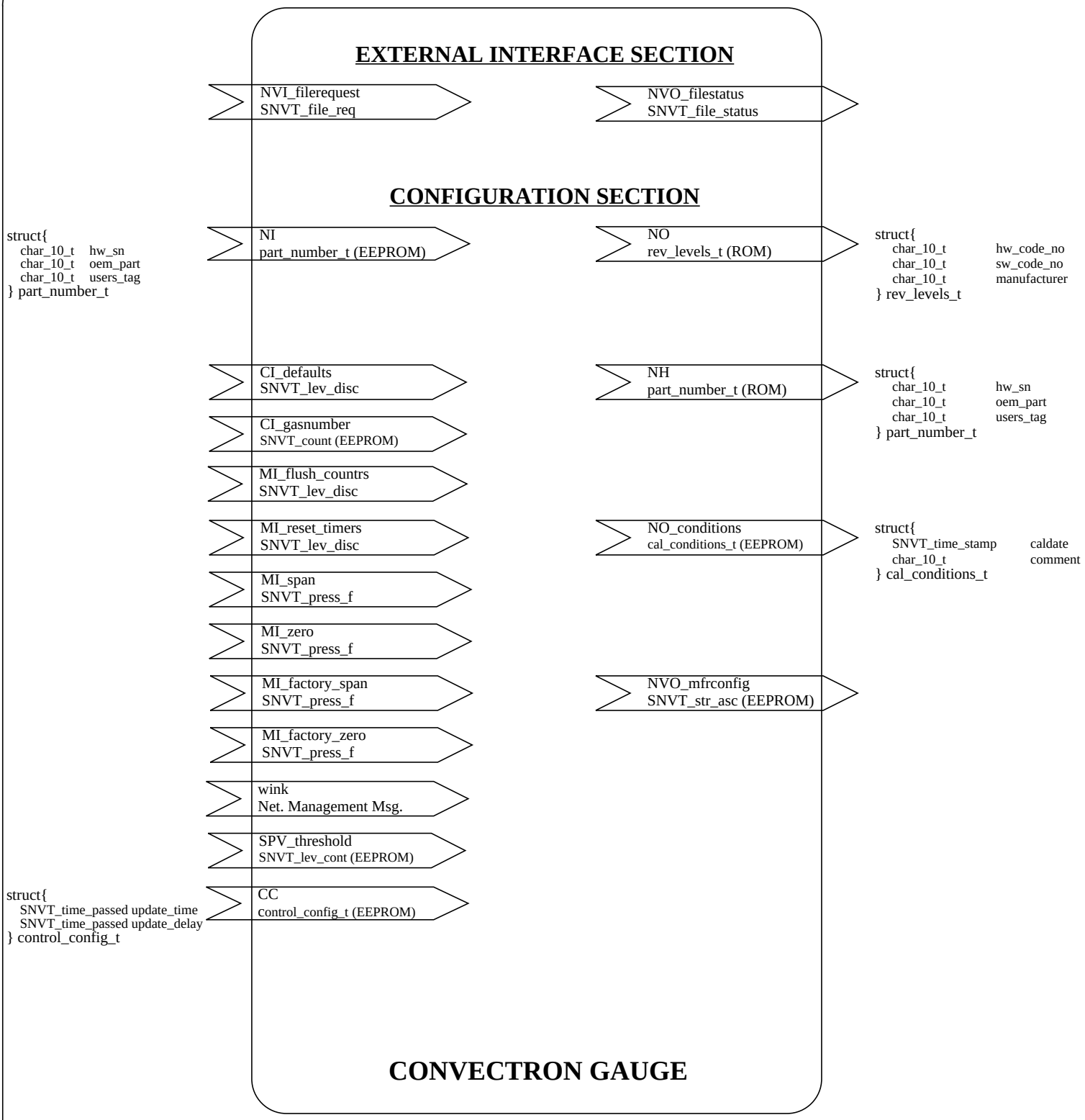

E. Aisawa DRAWN BY	10/13/97	**Sprite Pirani Gauge** **ERS** TITLE	HEWLETT PACKARD
E. Aisawa ENGINEER	10/13/97		
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REV	REVISIONS	APPROVED	DATE
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E. Aisawa DRAWN BY	10/13/97	**Sprite Ion Gauge** **ERS** TITLE	HEWLETT PACKARD
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N. Moreyra RELEASE TO PROD.	10/13/97		G1946-80005 PART NUMBER
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1.0 Ion Gauge Interface

The purpose of this document is to set forth the electrical and communication specifications for the ion gauge module that will be used in the Sprite instrument (G1946A). Since the ion gauge module has been designated as a non-real time subsystem module, the specifications for the communication interface will be governed by the Non-Real Time Subsystem (NRTS) ERS specification (A-G1946-90017-1). The network variables for the Ion Gauge will be defined in this specification.

1.1 Temperature and Humidity

The gauge module will be tested to Hewlett-Packard's standard tests for a Class B2 instrument with the following exceptions:

1.1.1 Minimum ambient operating temperature:15 deg C (tested to 10 deg C)

1.1.2 Maximum ambient operating temperature: 35 deg C (tested to 40 deg C)

1.2 EMC requirements

The ion gauge module will comply with all of the standards that the Sprite instrument will be held accountable for. The intent here is that the design team will not have to do anything special with the gauge module in order for the instrument to pass its tests.

1.3 Physical Connection

The gauge module will attach to the vacuum manifold via a NW16KF Stainless Steel flange.

1.4 Mains Power

The gauge module will derive all of its power from the Network connector and will necessarily be restricted by this fact.

1.5 Network Power

1.5.1 Current draw from the +24V DC lines on the network connector shall be less than 1 amp.

1.5.2 There should be sufficient isolation within the gauge module such that a failure within the module does not drag down the +24V supply lines.

1.6 Communication Connector

The controller will use a shielded 8 position, 8 contact RJ45 connector as shown in Figure 1.

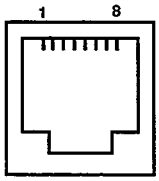


Figure 1: Ion Gauge Network Connector

1.6.1 Pin Definitions

1.6.1.1 Pin 1: +EIA485

1.6.1.2 Pin 2: -EIA485

1.6.1.3 Pin 3: Power Ground

1.6.1.4 Pin 4: +24 Volts

1.6.1.5 Pin 5: +24 Volts

1.6.1.6 Pin 6: Power Ground

1.6.1.7 Pin 7: Signal Ground

1.6.1.8 Pin 8: Reserved by Echelon Corporation

1.6.2 Wire gauge - 24 AWG minimum

1.6.3 Maximum current through any single pin is 1 Amp.

1.7 Bus Termination

The ion gauge should not have any internal terminations on the signal lines.

1.8 Installation

Refer to the NRTS ERS section, *Installation of subsystem elements.*

1.9 Interlocks

The ion gauge will have the following interlocks. The interlocks will be overridden by placing the gauge in its diagnostic mode.

1.9.1 Foreline pressure - If the foreline pressure is above a certain value (set by SPV_backpress), the gauge will not be allowed to turn on. Initial default is 100000 Pascal (near atmosphere).

1.9.2 Foreline pressure gauge communication - If the gauge does not receive repeatedly updated information from the foreline pressure gauge, the ion gauge will turn off and send a message to that effect. Default is 120 seconds for a communications fault with the foreline gauge.

1.10 Network Variable Inputs

1.10.1 *Mode [CI_mode]* - Enumerated type which tells a node whether to operate normally, perform a self test, or go into a diagnostic mode. Not all options need be implemented to used this variable.

1.10.1.1 Normal - default operation

1.10.1.2 Self_test - not used in Sprite

1.10.1.3 Ext_test - not used in Sprite

1.10.1.4 Diagnostic - Override interlocks

1.10.2 *Gauge OFF/ON [CI_on]* - Puts the gauge in its OFF or ON state. There are several different ON states as defined by the SNVT_lev_disc type.

1.10.2.1 ST_OFF - Gauge off

1.10.2.2 ST_LOW - Gauge on, filament at 0.1 ma emission

1.10.2.3 ST_MED - Gauge on, filament at 0.2 ma emission

1.10.2.4 ST_HIGH - Degas, filament at 10 ma emission

1.10.2.5 ST_ON - Gauge on, filament at 0.1 ma emission

1.10.3 *Foreline Pressure [CI_forepress]* - A floating point pressure number (SNVT_press_f) which represents the foreline pressure. The ion gauge expects periodic updates from this gauge and will turn off if it loses communication with the foreline gauge. The current timeout is 120 seconds.

1.10.4 *Event Selector [EI_event_select]* - A network variable that selects an event from the event log(s) (0 is the most recent event).

1.10.5 *System Date-Time [EI_sysdate]* - Sets the system date and time. This variable should be updated periodically (typically once a second).

1.10.6 *CI_filerequest [NVI_filerequest]* - Specifies to the device which file should be uploaded to the host.

1.10.7 *Part Number Information [NI]*

1.10.8 *Select Factory Defaults [CI_defaults]* - Restores the span calibration, the zero calibration, and the gasnumber to their factory set values.

1.10.9 *Gas Calibration Curve Selector [CI_gasnumber]* - Selects the gas curve the gauge is calibrated for.

1.10.10 *Flush Internal Timers [MI_flush_countrs]* - Immediately updates non-volatile timer memory.

1.10.11 *Reset Internal Timers [MI_reset_timers]* - Allows the module's internal timers to be reset.

1.10.12 *MI_span* - Variable for calibration

1.10.13 *MI_zero* - Variable for calibration

1.10.14 *MI_factory_span* - Variable for factory calibration

1.10.15 *MI_factory_zero* - Variable for factory calibration

1.10.16 *MI_ovp_setpoint* - Overpressure setpoint.

1.10.17 *NVI_sensitivity* - Allows for changing sensitivity variable. Factory default is 0.0414 and is used by the gauge manufacturer as a scaling factor in internal calculations.

1.10.18 *Foreline Pressure Setpoint [SPV_forepress]* - A floating point pressure number (SNVT_press_f) which will allow the end user to change the foreline pressure setpoint setting at which the ion gauge will be allowed to turn on. This setpoint will be stored in non-volatile memory. The current default setpoint is 100000 Pascal (near atmosphere pressure).

1.10.19 *Pressure Change Threshold [SPV_threshold]* - The percentage change in pressure above which would cause the module to override the update period and cause the pressure reading to be output immediately. This setpoint would be stored in non-volatile memory. Current default is 1% change will cause an output of a pressure reading to occur.

1.10.20 *wink* - Network management message. Node responds by flashing service pin indicator.

1.10.21 *Control Configuration [CC]*

The following structure field definitions are used by the manufacturer and the system integrator to stagger starting and stopping transients and network traffic in the situation where multi-

ple pumps are present. This information is accessible to anyone, is written into the node by the element's manufacturer and/or integrator, and is stored in non-volatile memory.

1.10.21.1 *Pressure Reporting Update Period [SPV_update_period]* - The amount of time allowed before a pressure reading is output. A change in pressure exceeding the threshold will be reported immediately, regardless of the status of the update period. This setpoint will be stored in non-volatile memory.

1.10.21.2 *Pressure Reporting Update Delay [SPV_update_delay]* - The amount of time after the expiration of the update period before a pressure reading is output. The purpose of this setpoint is to stagger pressure output readings from multiple gauges to avoid potential collisions. This setpoint will be stored in non-volatile memory.

1.11 Network Variable Outputs

1.11.1 *Status Information [SO]*

The following structure field definitions are used to communicate the status of an ion gauge.

1.11.1.1 *On-Off Status [on]* - This field communicates the ON-OFF state of the gauge.

1.11.1.2 *Warning Information [warn]* - This field is defined by the gauge manufacturer. The restriction here is that there are only 16 different warning conditions that can be reported in this variable.

1.11.1.3 *Shutdown Information [shutdown]* - This field has the same restriction as the Warning field.

1.11.2 *Pressure readout [SO_pressure]* - This variable reports the pressure reading from the gauge.

1.11.3 *Selected Gas Calibration Curve [SO_gas]* - This variable reports the gas that the gauge is calibrated for. Currently, there is only one gas that the gauge is calibrated for (Nitrogen).

1.11.4 *Service Output [MO]*

The following structure field definitions are used to extract maintenance information from the gauge. This information is stored in non-volatile memory.

1.11.4.1 *Total Time [total_time]* - This variable reports the total time that the gauge has been on.

1.11.4.2 *Process Time [total_proc]* - This field reports the total time that the gauge has been in its ON state.

1.11.4.3 *Service Time [serv_time]* - This field reports the approximate total ON time of the gauge to the next service.

1.11.4.4 *Process Service Time [serv_proc]* - This field reports the approximate process time of the gauge to the next service.

1.11.4.5 *Number of ON/OFF Cycles [cycles]* - This field reports the number of ON/OFF cycles that the gauge has undergone.

1.11.4.6 *Cycle Service Time [serv_cycles]* - This field reports the approximate number of ON/OFF cycles that the gauge has before the next service.

1.11.5 *Event Log Output Information [EO]*

The following structure field definitions are used to communicate a requested event log entry.

1.11.5.1 *Event Entry Retrieval from the On-Off Event Log [on_off_event]* - This field shows the on-off state from the requested event entry.

1.11.5.2 *Event Entry Retrieval from the Warning Event Log [warn_event]* - This field shows the Warning Status state from the requested event entry.

1.11.5.3 *Event Entry Retrieval from the Shutdown Event Log [shutdown_event]* - This field shows the Shutdown Status state from the requested event entry.

1.11.5.4 *System Date and Time Entry from Event Log [mark_event]* - This field shows the time that the requested event entry was logged.

1.11.6 *NVO_filestatus* - The device uses this network variable to inform the host of the status of the file transfer.

1.11.7 *Identification [NO]*

The following structure field definitions are used to identify the revision level and manufacturer of the ion gauge. This information is written into the node by the gauge's manufacturer, and is stored in non-volatile memory. These identification constants are directly readable as ASCII strings by polling the element.

1.11.8 *Hardware Identification [NH]*

1.11.9 *Subsystem Element Calibration conditions [NO_conditions]* - An optional network variable structure containing the following fields:

1.11.9.1 *System Date and Time [cal_date]* - This field shows the time that a calibration was performed.

1.11.9.2 *10 character ASCII string [comment]* - This field provides a place for a brief comment.

1.11.10 *Subsystem Element Configuration [NVO_mfrconfig]* - A manufacturer-optional designation which further defines the subsystem element's configuration. Expressed as a 30-character ASCII string.

1.12 Neuron® C Data Structures and Definitions

This section will repeat information found in the NRTS ERS document in order to have all the variable definitions for the Ion Gauge in one place.

Command	Refer to Section

```
typedef enum {
    normal      =0;
    self_test   =1;
    ext_test    =2;
    diagnostic  =3;
} control_mode;                                   NRTS ERS

network input control_mode CI_mode = normal;      NRTS ERS

network input
  sd_string ("ON/OFF state - (OFF,LOW-ON,HI-ON,DEGAS,LOW-
  ON).")
  SNVT_lev_disc CI_on = ST_OFF;                   1.10.2

network input
  sd_string ("Foreline pressure interlock reading. Initialized to 10^5
  Pascals.")
  SNVT_press_f CI_forepress = {0,71,67,20480};    1.10.3
  /* Initialized to 100,000 pascal */

network input
  sd_string ("Selects the event output on event out variables.")
  SNVT_count EI_event_select;                     NRTS ERS

network input
sd_string ("System Date and Time information")
SNVT_time_stamp EI_sysdate;                       NRTS ERS

network input SNVT_file_req NVI_filerequest       NRTS ERS
```

```
typedef struct {
        char_10         hw_sn;                  NRTS ERS
        char_10         oem_part;               NRTS ERS
        char_10         user_tag;               NRTS ERS
} part_number;

network input eeprom part_number NI;            NRTS ERS

network input
  sd_string ("Returns all SPV's and CI_gasnumber to their factory pre-
  set values.")
  config SNVT_lev_disc CI_defaults;             1.10.8

network input
  sd_string ("Selects the gas the gauge output is calibrated for. Gas
  numbers should be defined here.")
  config SNVT_count CI_gasnumber = 0;           1.10.9

network input
  SNVT_lev_disc MI_flush_countrs                1.10.10
network input
  sd_string ("ST_ON resets all internal counters and timers")
  SNVT_lev_disc MI_reset_timers = ST_OFF;       1.10.11

network input
  SNVT_press_f MI_span;                         1.10.12

network input
  SNVT_press_f MI_zero;                         1.10.13

network input
  SNVT_press_f MI_factory_span;                 1.10.14
```

network input
SNVT_press_f MI_factory_zero; 1.10.15

network input
SNVT_press_f MI_ovp_setpoint; 1.10.16

network input
SNVT_press_f NVI_sensitivity; 1.10.17

network input
sd_string (“Set Point Value, in Pascals, for the Ion Gauge foreline pressure interlock.”)
config SNVT_press_f SPV_forepress = {0,71,67,20480}; 1.10.18

network input
sd_string (“Set Point Value for the percentage change in pressure allowed above which the pressure will be reported immediately.”)
config SNVT_lev_count SPV_threshold = 2; 1.10.19

wink 1.10.20

typedef struct {
SNVT_time_passed update_period; 1.10.21.1
SNVT_time_passed update_delay; 1.10.21.2
} control_config;

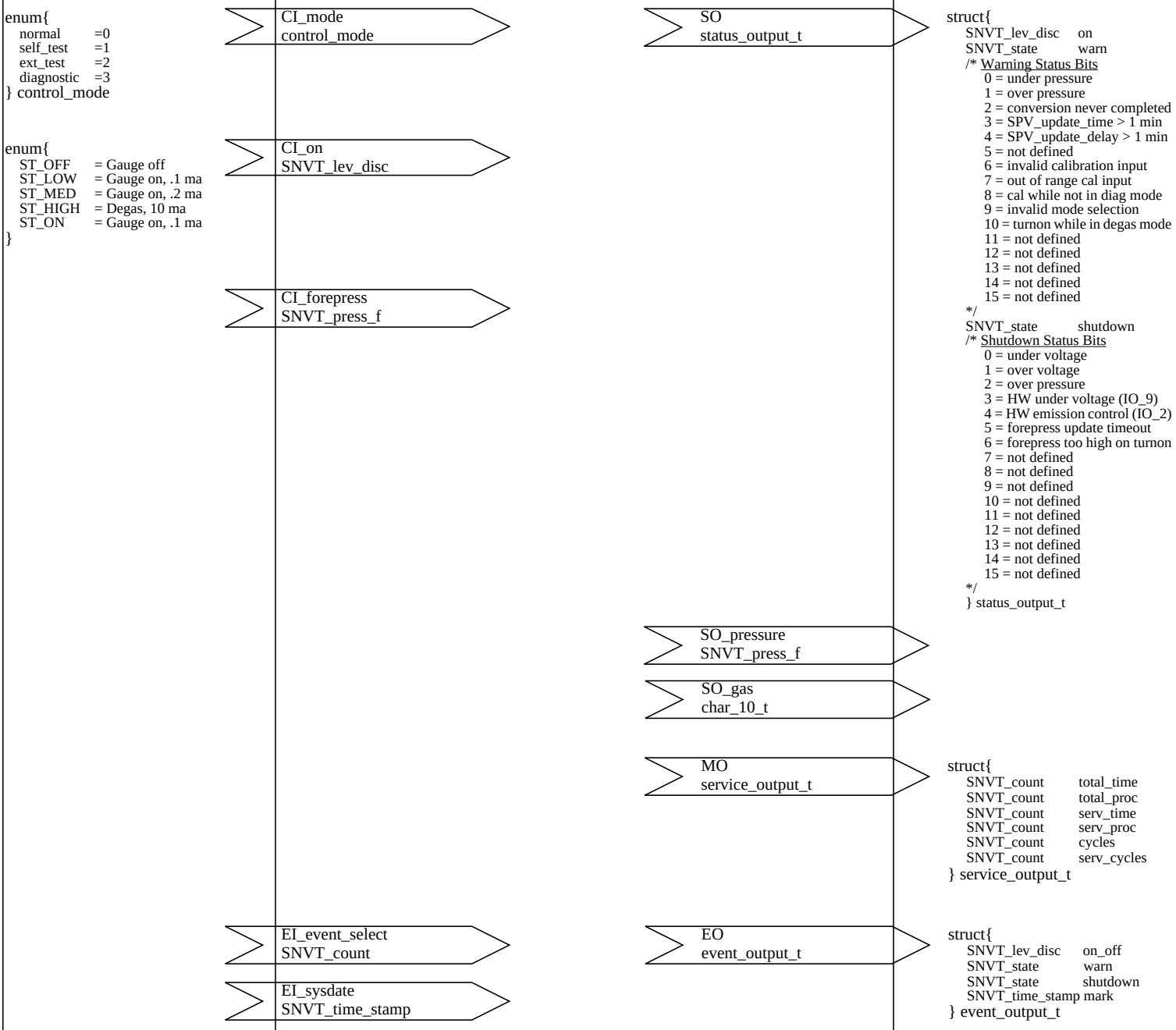
network input
config control_config CC = {0,0,2,0, 0,0,0,500}; 1.10.21

```
typedef struct {
    SNVT_lev_disc       on;                     NRTS ERS
    SNVT_state          warn;                   NRTS ERS
    /* Warning Status Bits
        0 = under pressure
        1 = over pressure
        2 = conversion never completed
        3 = SPV_update_time > 1 min
        4 = SPV_update_delay > 1 min
        5 = EI_event_select >= 4
        6 = invalid calibration input
        7 = out of range input
        8 = IO_0 hw over pressure
        9 = IO_9 hw under voltage
        10 = IO_2 hw emission shutdown
        11 = forepressure update timeout
        12 = turnon attempt in degas
        13 = invalid mode selection
        14 = not defined
        15 = not defined
    */
    SNVT_state          shutdown;               NRTS ERS
    /* Shutdown Status Bits
        0 = under voltage
        1 = over voltage
        2 = motor temp
        3 = not defined
        4 = not defined
        5 = not defined
        6 = not defined
        7 = not defined
        8 = not defined
        9 = not defined
        10 = not defined
        11 = not defined
        12 = not defined
        13 = not defined
        14 = not defined
        15 = not defined
    */
} status_output;
```

```
network output
  sd_string ("Pressure reading from gauge in Pascals.")
  SNVT_press_f SO_pressure;                                   1.11.2

typedef struct {
      char                ascii[10];
} char_10;

network output
  sd_string ("Name of Gas that the gauge output is calibrated for.")
  char_10 SO_gas;                                             1.11.3

typedef struct {
      SNVT_count          total_time;                         1.11.4.1
      SNVT_count          total_proc;                         1.11.4.2
      SNVT_count          serv_time;                          1.11.4.3
      SNVT_count          serv_proc;                          1.11.4.4
      SNVT_count          cycles;                             1.11.4.5
      SNVT_count          serv_cycles;                        1.11.4.6
} service_output;

network output service_output MO;                             1.11.4

typedef struct {
      SNVT_lev_disc       on_off;                             NRTS ERS
      SNVT_state          warn;                               NRTS ERS
      SNVT_state          shutdown;                           NRTS ERS
      SNVT_time_stamp     mark;                               NRTS ERS
} event_output;

network output event_output EO;                               NRTS ERS

network output SNVT_file_status NVO_filestatus                NRTS ERS
```

```
typedef struct {
        char_10             hw_code_no;                 NRTS ERS
        char_10             sw_code_no;                 NRTS ERS
        char_10             manufacturer;               NRTS ERS
} rev_levels;

network output
  const rev_levels NO =             {
                                    “0115-27103”,
                                    “PR11616115”,
                                    “       GP”
                                    };

typedef struct {
        char_10             hw_sn;                      NRTS ERS
        char_10             oem_part;                   NRTS ERS
        char_10             users_tag;                  NRTS ERS
} part_number_t;

network output const part_number_t NH =                 NRTS ERS
                                    {
                                    “Ion Gauge ”,               NRTS ERS
                                    "       OEM”,               NRTS ERS
                                    “Tag1.00.00”                NRTS ERS
                                    };

typedef struct {
        SNVT_time_stamp     caldate;                    NRTS ERS
        char_10             comment;                    NRTS ERS
} cal_conditions

network output eeprom cal_conditions NO_conditions      NRTS ERS

network output eeprom SNVT_str_asc NVO_mfrconfig        NRTS ERS
```

EXTERNAL INTERFACE SECTION



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EXTERNAL INTERFACE SECTION

NVI_filerequest
SNVT_file_req

NVO_filestatus
SNVT_file_status

CONFIGURATION SECTION

struct{
char_10_t hw_sn
char_10_t oem_part
char_10_t users_tag
} part_number_t

NI
part_number_t (EEPROM)

NO
rev_levels_t (ROM)

struct{
char_10_t hw_code_no
char_10_t sw_code_no
char_10_t manufacturer
} rev_levels_t

CI_defaults
SNVT_lev_disc

CI_gasnumber
SNVT_count (EEPROM)

NH
partnumber_t (ROM)

struct{
char_10_t hw_sn
char_10_t oem_part
char_10_t users_tag
} rev_levels_t

MI_flush_countrs
SNVT_lev_disc

MI_reset_timers
SNVT_lev_disc

NO_conditions
cal_conditions_t (EEPROM)

struct{
SNVT_time_stamp caldate
char_10_t comment
} cal_conditions_t

MI_span
SNVT_press_f

MI_zero
SNVT_press_f

MI_factory_span
SNVT_press_f

NVO_mfrconfig
SNVT_str_asc (EEPROM)

MI_factory_zero
SNVT_press_f

MI_ovp_setpoint
SNVT_press_f

NVI_sensitivity
SNVT_press_f

SPV_forepress
SNVT_press_f (EEPROM)

SPV_threshold
SNVT_lev_cont (EEPROM)

wink
Net. Management Msg.

struct{
SNVT_time_passed update_time
SNVT_time_passed update_delay
} control_config_t

CC
control_config_t (EEPROM)

ION GAUGE

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HEWLETT-PACKARD
California Analytical Division
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REV	REVISIONS	APPROVED	DATE
A	AS ISSUED PER PC23-6030	N. Moreyra	2/24/98

Turbo LON Interface Theory of Operation

1.0 Overview

The purpose of this document is to explain the design of the Turbo LON Interface Module (G1946-80007). This document will be split up into two major sections, the Hardware and the Firmware. Since the turbo pump has been designated as a non-real time subsystem module, the specifications for the communication interface will be governed by the Non-Real Time Subsystem (NRTS) ERS specification (document A-G1946-90017-1). See the document A-G1946-80007-8 for the complete description of the communication interface.

2.0 Hardware

The hardware was designed by Edwards High Vacuum to connect to our NRTS system and be able to control two turbomolecular pumps that are powered with Edwards EXDC family of controllers. The design requires a separate power supply to provide the power for the controllers (Sprite uses a 75VDC power supply). It also assumes the communication connector is as specified in the NRTS Specification document A-G1946-90017-1.

2.1 Connections to the Outside World

There are four connectors on the interface module. There is also a stud which is intended to be the safety ground for the module. This stud must be connected to the Earth ground of the Turbo pump power supply.

2.1.1 Controller 1 - This is a 9 pin D-Sub connector (Female) which is intended to connect to the EXDC family turbo controller (Sprite uses an EXDC160 for controller 1). The pin connections are defined by the Edwards manual for the EXDC controller family.

2.1.1.1 Pin 1: Start - Controller ON/OFF signal, Low is pump on

2.1.1.2 Pin 2: Normal - Indicator for >80% speed, Low means speed >80%

2.1.1.3 Pin 3: Earth- Safety Ground

2.1.1.4 Pin 4: Speed - Analog signal from controller, 0-10V represents 0-100% speed

2.1.1.5 Pin 5: PS Return - Power Return from the controller

2.1.1.6 Pin 6: PS Return - Power Return from the controller

2.1.1.7 Pin 7: PS Out - Power Out to controller

2.1.1.8 Pin 8: PS Out - Power Out to controller

2.1.2 Controller 2 - This is a 9 pin D-Sub connector (Female) which is intended to connect to the EXDC family turbo controller (Sprite uses an EXDC80 for controller 2). The pin connections are defined by the Edwards manual for the EXDC controller family and are the same as defined in the above section.

2.1.3 Communication - The module will use a shielded 8 position, 8 contact RJ45 connector as shown in Figure 1 for digital communication. The 24 Volt supply is used to generate the +/-5 Volts that is used within the module.

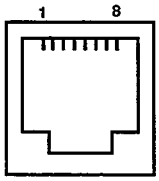

Figure 1: Turbo Controller Network Connector

2.1.3.1 Pin Definitions

2.1.3.1.1 Pin 1: +EIA485

2.1.3.1.2 Pin 2: -EIA485

2.1.3.1.3 Pin 3: Power Ground

2.1.3.1.4 Pin 4: +24 Volts

2.1.3.1.5 Pin 5: +24 Volts

2.1.3.1.6 Pin 6: Power Ground

2.1.3.1.7 Pin 7: Signal Ground

2.1.3.1.8 Pin 8: Reserved by Echelon Corporation

2.1.3.2 Maximum current through any single pin is 1 Amp.

2.1.4 Power Supply Input - A 9-pin Male D-sub connector which brings power from an external supply to the module. This supply is the raw supply that is directed to the EXDC controllers and must meet the requirements for the EXDC controller family.

2.1.4.1 Pin 1: Not Connected

2.1.4.2 Pin 2: Not Connected

2.1.4.3 Pin 3: Not Connected

2.1.4.4 Pin 4: - Supply

2.1.4.5 Pin 5: - Supply

2.1.4.6 Pin 6: - Supply

2.1.4.7 Pin 7: + Supply

2.1.4.8 Pin 8: + Supply

2.1.4.9 Pin 9: + Supply

2.1.5 Ground Stud - This stud is connected to the metal case of the module. It is intended to be the connection point for an 18 AWG Green/Yellow wire that connects the module's case to the earthing stud on the turbo controller power supply. Although there is a shielded cable between the module and the power supply, the shield cannot be used as a safety ground.

2.2 Measured Turbo Parameters

There are six directly measured parameters in the module. One of the parameters supplied by the EXDC controllers that is not used is the NORMAL signal. Monitoring this signal is not necessary since we monitor the controller's speed line.

2.2.1 CONTROLLER1_CURRENT - This parameter represents the current that goes through the EXDC controller that connects to the Controller1 connector (EXDC160 for Sprite). It is measured by putting a 0.1 ohm resistor between ground and the -SUPPLY pins of the Controller1 connector. The voltage across the resistor will be proportional to the current going through the controller. The current is used for the power calculation of controller1

2.2.2 CONTROLLER2_CURRENT - This parameter represents the current that goes through the EXDC controller that connects to the Controller2 connector (EXDC80 for Sprite). It is measured in a way identical to the measurement of the controller1 current. The current is used for the power calculations for controller2.

Note: Care must be taken in the layout of the CONTROLLER1_CURRENT and CONTROLLER2_CURRENT lines. With the amount of current that could go through these lines, significant errors could be built up through the voltage drop along printed circuit traces.

2.2.3 80V_Signal - This is the signal that is proportional to the supply voltage being delivered to the module. It is measured as the output of a resistor divider circuit (120K ohm and 680 ohm) and is used in the power calculations for both turbos.

2.2.4 ASPEED2_SIGNAL: This is a signal that measures the speed of Controller2. It is measured by haveing a resistor divider (10K ohm and 1K ohm) attached to the ASPEED pin of the controller2 connector. On the incoming signal 0-10V corresponds to 0-100% speed.

2.2.5 ASPEED1_SIGNAL: This is a signal that measures the speed of Controller1. It is measured by haveing a resistor divider (10K ohm and 1K ohm) attached to the ASPEED pin of the controller1 connector. On the incoming signal 0-10V corresponds to 0-100% speed.

2.2.6 OV_REFERENCE - This is a measurement that is performed to subtract off any ground offsets due to the A/D converter. This is necessary to improve the accuracy of the data acquistion because all inputs to the A/D converter need to be divided down to a +/0.5 Volt window (ADC input restriction).

2.3 Analog to Digital Conversion

The communication processor (Neuron 3150) coordinates the data acquisition process. The parameters to be measured form the inputs to an 8 to 1 Analog Multiplexor (MUX) that feeds the A/D converter (Maxim MAX132).

The MAX132 is a +/-18 bit Analog to Digital Converter with a serial interface. Its data sheets can be found in Maxim's 1993 New Releases Data Book, Volume 2. The ADC has a programmable port that the communication processor writes to. The port selects which MUX channel is to be measured. Although a wider range is allowed, the input to the ADC is limited to a +/-512mV window to guarantee performance over the entire input range.

After selection of a channel to be measured, the communication processor initiates a measurement. After the conversion is completed, the communication processor reads the data and converts the reading into a pressure.

2.4 Communication Processor

The communication processor is from Echelon Corporation, is manufactured by Toshiba, and is called a Neuron Model 3150. This processor implements the protocol that the Sprite NRTS utilizes. For more information, please refer to the NRTS General Specification (A-G1946-90017-1).

3.0 Firmware

The first version of firmware was specified by Hewlett Packard and written by Edwards High Vacuum. Later, the responsibility for the code was transferred to Hewlett Packard. This section will give an overview of how the code functions. For exactly what interface variables are implemented, please see document A-G1946-80007-8.

3.1 Overview

The firmware for this module runs on Echelon Corporation's Neuron 3150. As such it is written in a language called Neuron C. The Neuron runs code in an event driven manner using a round robin

scheduler. The firmware for the module makes heavy use of timers to dictate when actions are to take place. Other events occur as a result of receiving network variables.

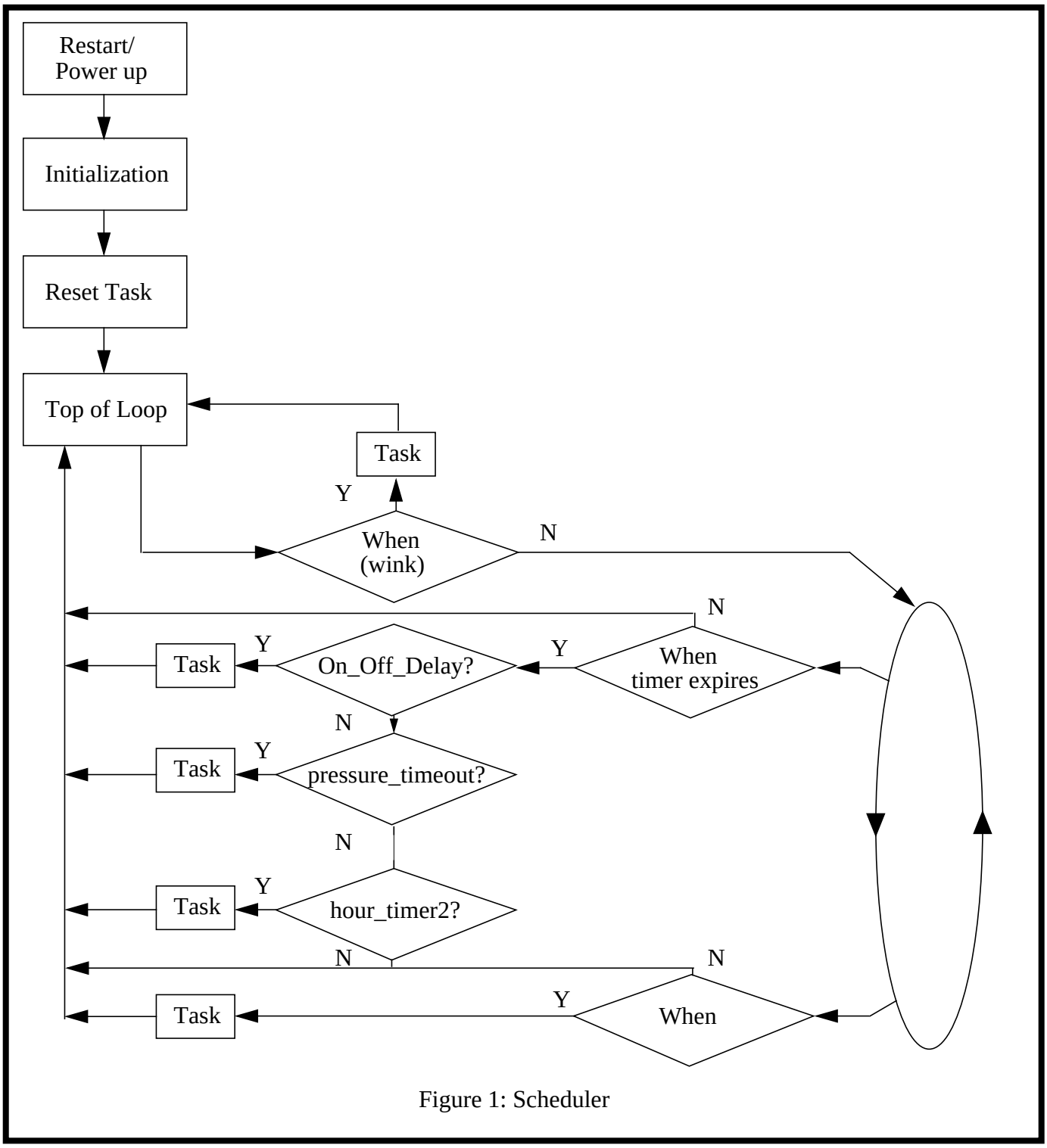

Figure 1: Scheduler

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3.2 Timers

3.2.1 On_Off_Delay - This is a millisecond timer that runs the state machines for the two turbo pumps and the vacuum system. Pump states are based on pump speed and the state of the CI_on network variable (on/off command). The vacuum state is based on the pump states and the CI_on variable.

3.2.1.1 Turbo Pump 1 States.

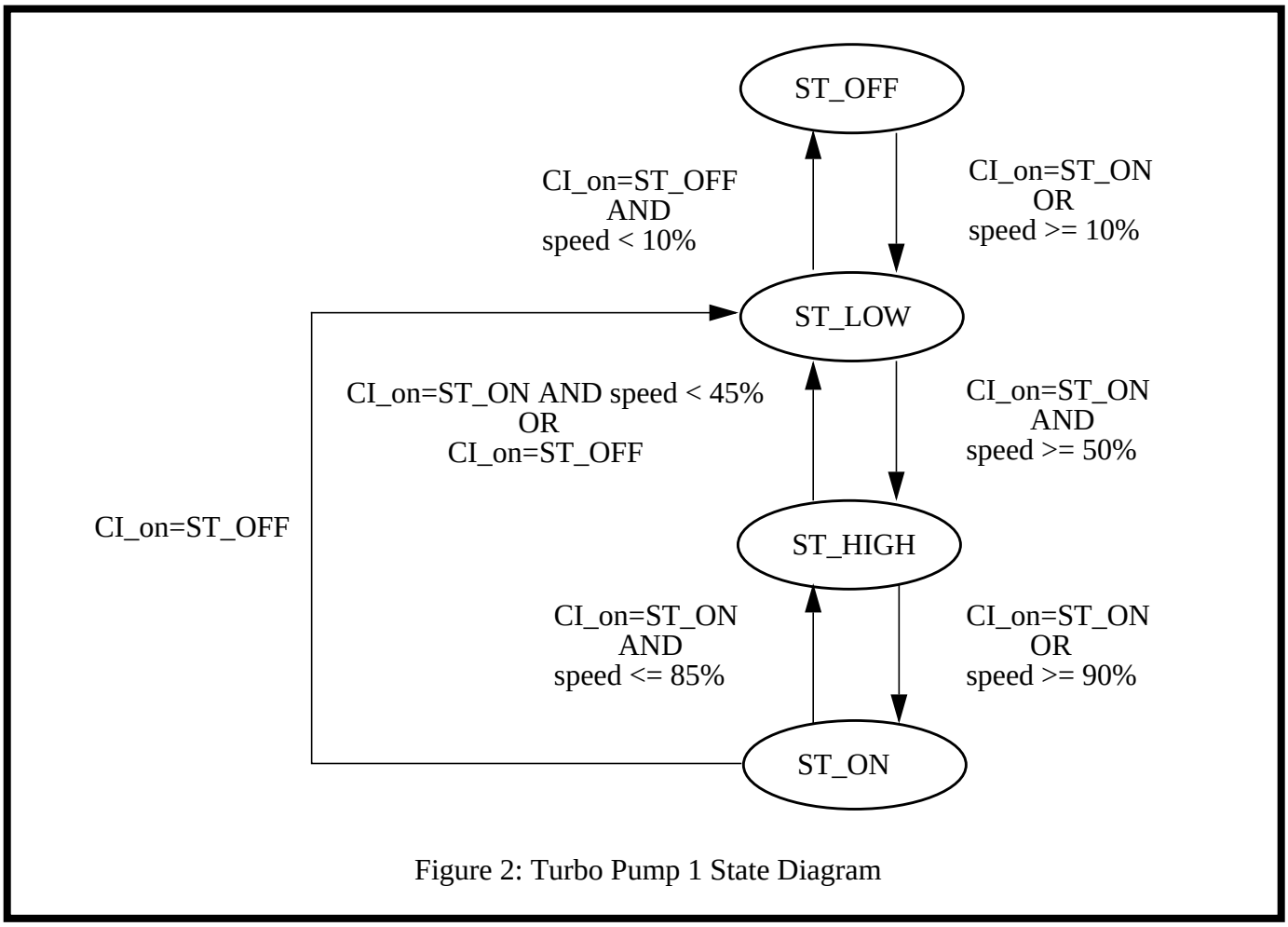

Figure 2: Turbo Pump 1 State Diagram

3.2.1.1.1 ST_OFF - Speed is 0 and CI_on is ST_OFF. There is a zero threshold limit implemented in firmware. If the measure speed is less than 10%, the speed is set to zero.

3.2.1.1.2 ST_LOW - Speed is less than 50% and CI_on is ST_ON, or speed is greater than 10% and CI_on is ST_OFF.

3.2.1.1.3 ST_MED - Not Used

3.2.1.1.4 ST_HIGH - Speed is between 50% and 90% and CI_on is ST_ON.

3.2.1.1.5 ST_ON - Speed is greater than 90% and CI_on is ST_ON.

3.2.1.2 Turbo Pump 2 States

3.2.1.3 Turbo 2 is not turned on until turbo 1 has reached its ST_ON state. If ever turbo 1 falls out of this state, turbo 2 is turned off.

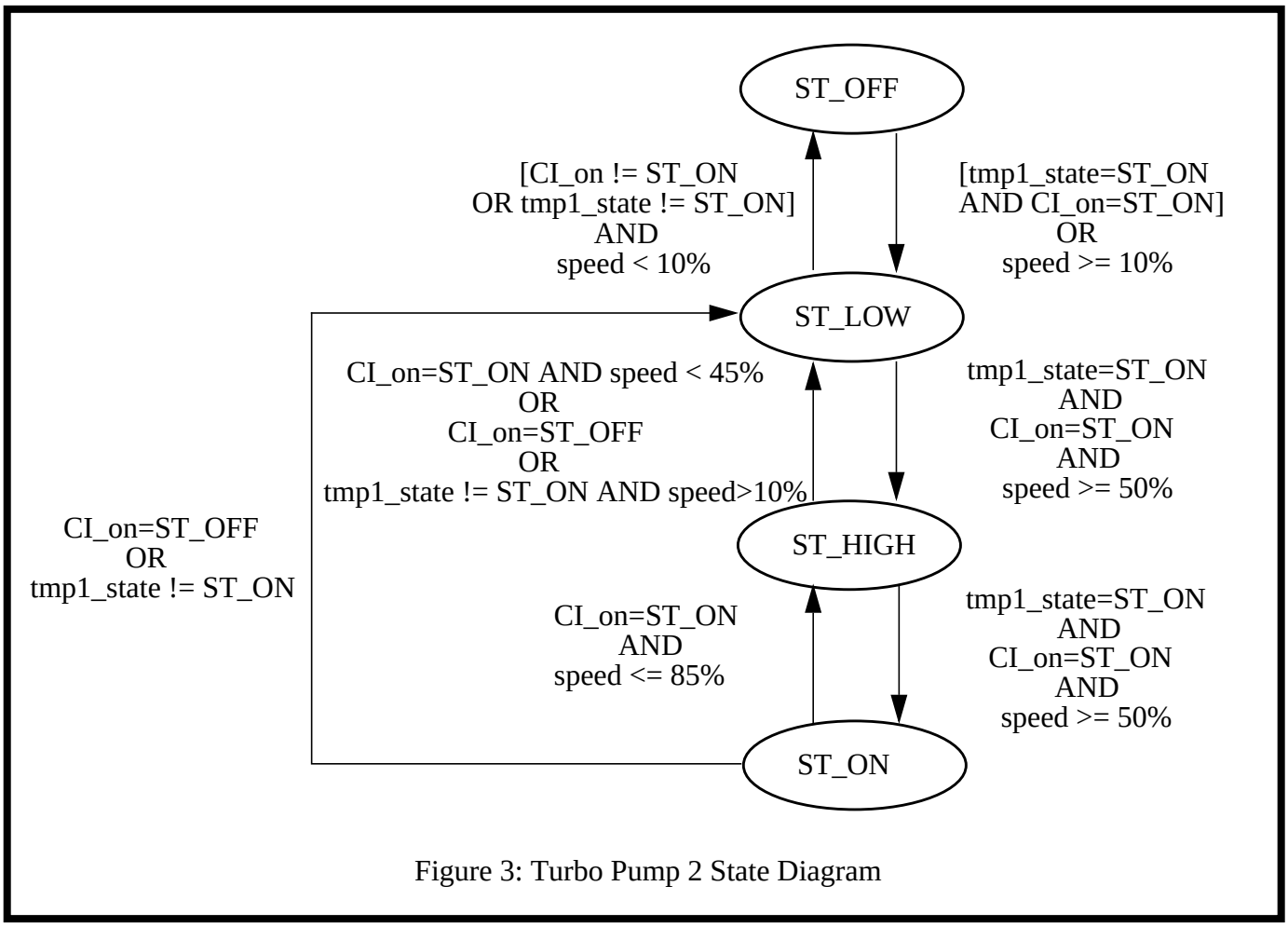

Figure 3: Turbo Pump 2 State Diagram

3.2.1.3.1 ST_OFF - Speed is 0 and CI_on is ST_OFF. There is a zero threshold limit implemented in firmware. If the measured speed is less than 10%, the speed is set to zero.

3.2.1.3.2 ST_LOW - Speed is less than 50% and CI_on is ST_ON, or speed is greater than 10% and CI_on is ST_OFF.

3.2.1.3.3 ST_MED - Not Used

3.2.1.3.4 ST_HIGH - Speed is between 50% and 90% and CI_on is ST_ON.

3.2.1.3.5 ST_ON - Speed is greater than 90% and CI_on is ST_ON.

3.2.1.4 Vacuum System State

The state machine for the vacuum system performs the power-on sequence of the turbo pumps. Sprite uses a 200 watt power supply for the EXDC controllers. If the firmware turned both controllers on at the same time, the power draw would exceed the capacity of

the supply. Instead, the firmware turns on controller 1 first, waits until its speed reaches 90%, and then turns on controller 2.

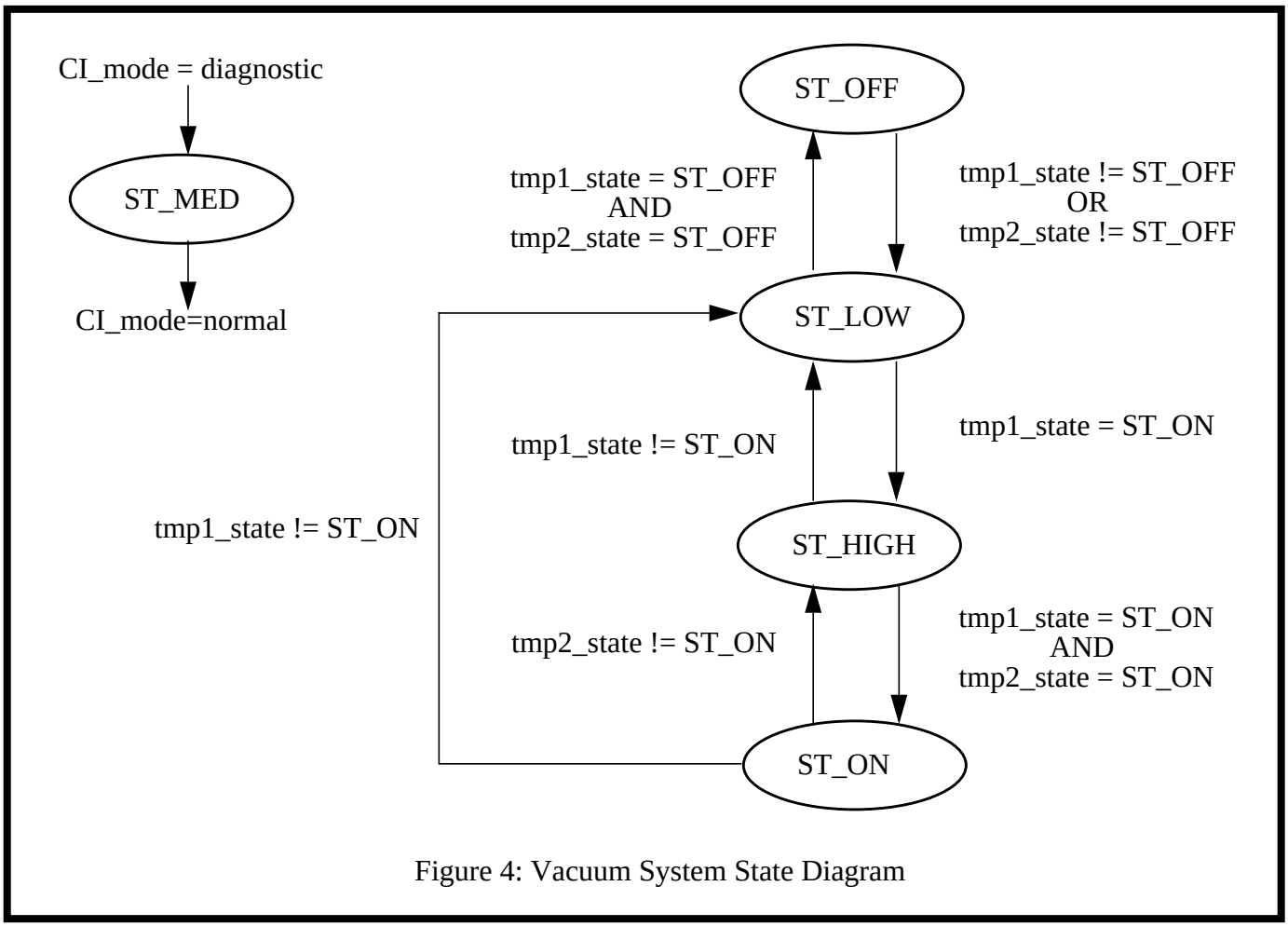

Figure 4: Vacuum System State Diagram

3.2.1.4.1 ST_OFF - Both pumps are at zero speed and CI_on is ST_OFF

3.2.1.4.2 ST_LOW - Controller 1's speed is less than 90% and CI_on is ST_ON, or either controller's speed is greater than zero and CI_on is ST_OFF. In this state, controller 2 is turned off independent of the state of CI_on. If CI_on is in state ST_ON, controller 1 is turned on.

3.2.1.4.3 ST_MED - This indicates that the turbo LON module is in its diagnostic state. This state is reached with the CI_mode network variable. When CI_mode is set to DIAGNOSTIC, this state is reached. Being in this state disables all the protection for the pumps. This allows the turbos to be turned on in any order without regard to foreline pressure. As such, this mode should only be entered by individuals who know what they are doing. Upon leaving this state, the values of tmp1_state, tmp2_state, and CI_on will determine what state the vacuum jumps to.

3.2.1.4.4 ST_HIGH - Controller 1's speed is greater than 90% and CI_on is in state ST_ON. Controller 2 is turned on here.

3.2.1.4.5 ST_ON - Both controllers are at greater than 90% speed and CI_on is ST_ON. This is the state where the stage 4 ion gauge is turned on. The gauge is turned off if the vacuum system falls out of this state.

3.2.2 Pressure_Timeout - This timeout is used for checking communication with the foreline gauge. The foreline gauge typically outputs a pressure once a second. If the timer expires, it is assumed that the module has lost communication with the foreline gauge and the turbo pumps are shut down until communication is restored. The timer is always reset upon each received pressure reading from the foreline gauge.

3.2.3 Forepress_Timer - This timer is used as a software debounce for the foreline pressure reading to the module. This was installed to handle an anomaly we occasionally saw with the foreline gauge. Once the foreline pressure has fallen below the point where the turbos have been turned on, this timer goes active if a pressure reading is detected that would turn the pumps off. If the high reading still persists on the expiration of the timer, the pumps are turned off.

3.2.4 IG_Timeout - This timer performs a function similar to the Pressure_Timeout timer except for the stage 4 ion gauge. The timer is always reset upon each received pressure reading from the ion gauge (typically once a second). The only effect of lost ion gauge communication is to set a status bit.

3.2.5 IG_Poll_Timer - This timer, upon expiration, polls the stage 4 ion gauge for its status. The reason for doing this is to monitor the ON/OFF state of the gauge. In the event the ion gauge is unplugged and plugged back in, the module can tell if the gauge is off and then turn it back on. The timer is always reset after expiration.

3.2.6 SpdPwr_Update_Timer - This timer, upon expiration, propagates the speed and power variables for the two turbo pumps. Since network variables typically don't propagate themselves unless they change value, pump speed could potentially reach a state where its value would not change (e.g. 100%). Sprite is set up so that it is possible to turn the electronics off while keeping the vacuum system alive. When the electronics are brought up again, it's possible that the speed parameters on the SICB-LON Adaptor board (G1946-60007) may not get updated. This timer makes sure that the module's parameters get periodically output. After expiration, the timer is always reset.

3.2.7 ADC_Conversion - This timer goes into effect at the start of an ADC conversion. The time was chosen to be just slightly longer than the maximum guaranteed conversion time for the MAX132 ADC. Upon expiration, the ADC value is retrieved and another measurement is set up and started (as well as resetting this timer).

3.2.8 Pumpdown_Timer - This timer is a check to see if a turbo pump reaches 50% speed within a reasonable period of time. The timer is cleared once the pump has reached 50% speed. If the timer expires, the pumps are shut down and a status bit is set.

3.2.9 Vent_Check1_Timer - This timer is a delay timer. It is set when controller 1 is turned off. Upon expiration, a flag is set which will enable speed checking for the vent. Turbo 1's speed much continously decrease to avoid any error.

3.2.10 Vent_Check2_Timer - This timer is a delay timer. It is set when controller 2 is turned off. Upon expiration, a flag is set which will enable speed checking for the vent. Turbo 2's speed much continously decrease to avoid any error.

3.2.11 Diag_Delay_Timer - This timer is a delay timer. It is set when a pump is turned on. Upon expiration, diagnostic checks for the pump are enabled. The delay is necessary because there is some delay until the reported speed reading goes above 0% due to a speed threshold implemented in firmware (any speed under 10% gets reported as 0%). Since the turbos are turned on sequentially, this same timer is used for both pumps.

3.2.12 Hour_timer1 - This timer is used to help log the number of hours that turbo 1 has been on. It is set when turbo 1 is turned on. Upon expiration, the counter for the hours that turbo 1 has been on is updated and the timer is reset.

3.2.13 Hour_timer2 - This timer is used to help log the number of hours that turbo 2 has been on. It is set when turbo 2 is turned on. Upon expiration, the counter for the hours that turbo 2 has been on is updated and the timer is reset.

3.3 Data Acquisition

As mentioned in the hardware section, data is acquired by setting a channel on an analog multiplexor, triggering the ADC, read the ADC, and start another acquisition cycle. A timer is used to wait for the ADC to complete its conversion before processing the data and starting another conversion. Utilizing the end-of-convert signal from the ADC as an event trigger was disasterous. It just didn't work reliably (perhaps too much noise on the board). Waiting the maximum time for a conversion worked very reliably and that is what is used in the code.

3.3.1 Analog to Digital Conversion

This was accomplished through the use of functions written by Edwards High Vacuum to interface with the MAX132 analog to digital converter. Sprite used these functions exactly as written to do the A/D conversions.

3.3.1.1 Read_ADC_count() - This function returns a signed long integer. The top 15 bits are read from the 18-bit MAX132 ADC and returned.

3.3.1.2 Subtract zero channel reading (subtract offset).

3.3.1.3 Convert_Count_Volts(adc_count) - This function converts the adc_count to a voltage reading (units of tenths of millivolts).

3.3.1.4 Manipulate data - Do whatever manipulation is necessary to transform the ADC reading to units meaningful for the measurement (e.g. multiply by a scaling factor to undo the scaling from a resistor divider network).

3.3.1.5 Start_Conversion(next_channel) - Set up the next channel to be converted, wait 5 msec, and then trigger the conversion.

3.3.2 Channel order - Figure 4 shows the order in which measurements are made.

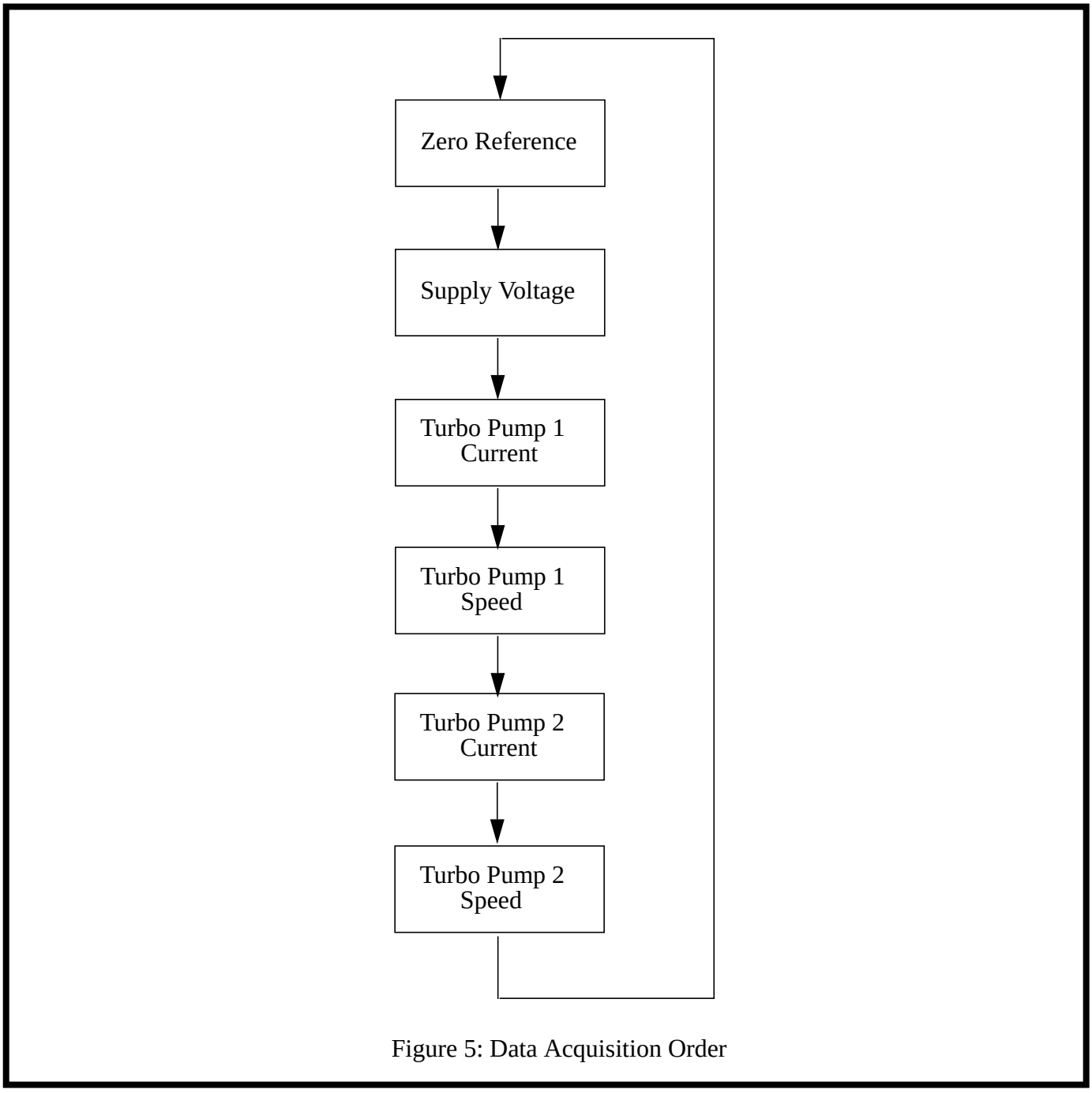

Figure 5: Data Acquisition Order

3.3.2.1 Zero Reference - Channel 2 of the MUX is used for this reading. The purpose of this reading is to get the ADC offset counts for a zero input to the MUX. This reading will be subtracted off the other measurements.

3.3.2.2 Supply Voltage - This is measured from channel 5 of the MUX. This value is used to check to make sure the supply is within the specifications of the EXDC controllers and is also used for the power consumption calculations for the two controllers.

3.3.2.3 Turbo Pump 1 Current - This is measured from channel 7 of the MUX. This value is used, along with the supply voltage reading, to determine the power consumption of controller 1. It is also used as a diagnostic. If the reading is zero when the pump is supposed to be on, a status event is recorded that there is low power for pump 1. The most likely reason for this event is that the controller is not plugged into the module.

3.3.2.4 Turbo Pump 1 Speed - This is measured from channel 4 of the MUX. This value is used to report the speed back to the data system (0-100%). It is also used as a diagnostic. If the pump is supposed to be on and power is being consumed by the controller and the speed is zero, a status event is recorded that there is a pump fault. This could be caused by a siezed rotor on the turbo pump.

3.3.2.5 Another event that could cause this error to occur is if the EXDC controller was reporting an incorrect speed. Speed readings have been seen much lower than the actual speed in faulty EXDC controllers. When the pump is turned on, the reported speed was still zero when the diagnostic delay timer expired and a fault was generated. The controller was reporting the speed too low (actually half the actual speed) and that, coupled with the threshold of 10% before a non-zero speed would be reported, was enough to delay the zero speed reading past the diagnostic timer expiration and a fault would be generated. The faulty speed reading meant the pump would have had to reach 20% speed before the delay timer expired to have avoided this fault.

3.3.2.6 Turbo Pump 2 Current - This is measured from channel 6 of the MUX. This value is used, along with the supply voltage reading, to determine the power consumption of controller 2. It is also used as a diagnostic. If the reading is zero when the pump is supposed to be on, a status event is recorded that there is low power for pump 2. The most likely reason for this event is that the controller is not plugged into the module.

3.3.2.7 Turbo Pump 2 Speed - This is measured from channel 3 of the MUX. This value is used to report the speed back to the data system (0-100%). It is also used as a diagnostic. If the pump is supposed to be on and power is being consumed by the controller and the speed is zero, a status event is recorded that there is a pump fault. This could be caused by a siezed rotor on the turbo pump or by a faulty controller as explained previously.

3.4 Diagnostics

The Turbo LON Interface Module has a number of real time diagnostics and maintenance information. The diagnostic information is primarily contained in the module's electronic log book and its status output variable. The maintenance information contains information as to how long a pump has been on and how many on/off cycles it has been through.

3.4.1 Electronic Log Book

The Electronic Log Book for this module is stored in EEPROM on the Neuron. There is a limit of 10 entries. If there are more than 10 entries, the oldest entry is overwritten. An entry

of a log entry is a snapshot of the Shutdown status bits, turbo speed and power, and the foreline pressure.

3.4.1.1 EI_event_select - This variable is used to request a log entry to be output. The effective range of this variable is 0 - 9. Any entry greater than 9 will just return entry 9. The entries are ordered with entry 0 being the most recent entry and 9 is the oldest entry.

3.4.1.2 EO - This is the output variable which contains the requested log book entry.

3.4.2 Status Output Network Variable

The status output network variable is a 16 bit data structure. The fields are labelled bit0 thru bit15. See the document A-G1946-80007-8 for a complete listing of the module's network variables and types.

3.4.2.1 Vacuum System State - The states have been presented earlier.

3.4.2.2 Warning Bits

These bits relay information about the status of the pumps. The setting of these bits do not result in the turnoff of the controllers.

3.4.2.2.1 Bit0 - Bit9: These bits report the states for the two turbo pumps. The definition of the states has been covered earlier.

3.4.2.2.2 Bit10: This bit is set if the turbo supply voltage falls below 65V.

3.4.2.2.3 Bit11: This bit is set if the module is in its Diagnostic Mode.

3.4.2.2.4 Bit12: This bit is set if, after the diagnostic delay timer has expired, the current reading for controller 1 is zero and controller 1 is on.

3.4.2.2.5 Bit 13: This bit is set if, after the diagnostic delay timer has expired, the current reading for controller 2 is zero and controller 2 is on.

3.4.2.2.6 Bit14: This bit is set if communication is lost with the ion gauge (no update from the ion gauge for 30 seconds).

3.4.2.2.7 Bit15: Not defined

3.4.2.3 Shutdown Bits

The setting of any of these bits will result in the module trying to shut down the controllers. Some of these conditions are correctable and the module will resume normal operation with the removal of the condition that set the bit.

3.4.2.3.1 Bit0 - Bit7: Not defined

3.4.2.3.2 Bit8: This bit is set if controller 1 does not reach 50% speed in a time specified by the SPV_ControlParms.secsTo50 network variable. The default is 600 seconds (10 minutes). This results in a non-recoverable shutdown.

3.4.2.3.3 Bit9: This bit is set if controller 2 does not reach 50% speed in a time specified by the SPV_ControlParms.secsTo50 network variable. The default is 600 seconds (10 minutes). This results in a non-recoverable shutdown.

3.4.2.3.4 Bit10: This bit is set if, after the expiration of the diagnostic delay timer, there is non-zero power being consumed by controller 1 and the speed is zero. This results in a non-

recoverable shutdown. Although this fault may be reported as a pump failure, it is possible that the fault is due to a faulty speed line on the EXDC controller. Before concluding that this fault is a pump fault (siezed rotor), cycle power and verify that the red LED's on the EXDC controller stay in one state (only one red LED should be on if the rotor is not rotating).

3.4.2.3.5 Bit11: This bit is set if, after the expiration of the diagnostic delay timer, there is non-zero power being consumed by controller 2 and the speed is zero. This results in a non-recoverable shutdown.

3.4.2.3.6 Bit12: This bit is set if, after the expiration of either the vent_check1 timer or the vent_check2 timer, it is detected that the turbo speeds are not decreasing. This results in a non-recoverable (attempted) shutdown.

3.4.2.3.7 Bit13: Not defined

3.4.2.3.8 Bit14: This bit is set if the module does not receive a pressure reading from the foreline pressure gauge in 30 seconds. This results in a recoverable shutdown. Once updates are being received, the module clears this bit and resumes normal operation.

3.4.2.3.9 Bit15: This bit is set if the module receives a pressure reading from the stage 1 foreline gauge that the foreline pressure is above the value set by SPV_backpress. The default is 750 Pascal. This results in a recoverable shutdown. Once the pressure goes below SPV_backpress, the bit is cleared and the module resumes normal operation.

3.4.2.4 Diagnostic Mode

This is a mode that the module can be put into by setting CI_mode to DIAGNOSTIC. This mode disables all the protections from the controllers. Pumps can be turned on without the presence of a foreline gauge. This mode should only be used by trained personnel.

By entering diagnostic mode, the T2_on variable is enabled. This is the variable used to turn the pumps on and off.

3.4.2.4.1 ST_OFF: Both controllers are turned off.

3.4.2.4.2 ST_LOW: Controller 2 is turned on.

3.4.2.4.3 ST_MED: Not used

3.4.2.4.4 ST_HIGH: Controller 1 is turned on.

3.4.2.4.5 ST_ON: Controller 1 and 2 are turned on. Caution: The turbo power supply cannot supply enough power to support both controllers on at the same time for a cold start.

3.4.2.5 Maintenance

The maintenance variables keep track of hours of operation for the two turbos. To properly make use of the maintenance information, there are input variables that must also be used to keep the maintenance information correct.

3.4.2.5.1 MO1 - This structure keeps track of the number of hours of operation and the number of on/off cycles of turbo 1.

3.4.2.5.2 MO2 - This structure keeps track of the number of hours of operation and the number of on/off cycles of turbo 2.

3.4.2.5.3 MI_flush_countrs - This variable is used to sweep the maintenance information into non-volatile memory. This should always be done after every vent or before the instrument is powered off. The hour counters are only transferred to non-volatile memory every 10 hours of operation. This was done to minimize the number of writes to EEPROM (which has a limited write life time).

3.4.2.5.4 MI_reset_timers1 - This variable zeroes the counters for turbo 1. This should be used if turbo 1 is replaced.

3.4.2.5.5 MI_reset_timers2 - This variable zeroes the counters for turbo 2. This should be used if turbo 2 is replaced.

3.5 Miscellaneous

3.5.1 Autopumpdown - This is a variable that is stored in non-volatile memory. The state of this variable determines whether the module automatically starts sequencing the pumps on at power up. By default, the module will always pump down on power up. This was implemented to assist during troubleshooting in the case where a person would not want the pumps to come on.

3.5.2 Ion Gauge Communication

3.5.2.1 IG_SO - This variable communicates the status of the stage 4 ion gauge to the module. The on/off status of the ion gauge is what is of interest to the module.

3.5.2.2 IG_pressure - This variable is used as a communication heartbeat.

3.5.2.3 Ion_Gauge_ON - This variable is used to turn on the ion gauge. The gauge is turned on when the vacuum state is in its ST_ON state.

3.5.3 NO - This variable provides information on the module's hardware and firmware revs. There is also a place to state the manufacturer of the module.

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REV	REVISIONS	APPROVED	DATE
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E. Aisawa DRAWN BY	10/13/97	**+/-5KV HIGH VOLTAGE CURRENT SOURCE SPECIFICATION** TITLE	HEWLETT PACKARD
E. Aisawa ENGINEER	10/13/97		
N. Moreyra RELEASE TO PROD.	10/13/97		G1946-80014 PART NUMBER
SUPERSEDES DWG.	CURRENT REV A	PAGE 1 OF 4	**A-G1946-80014-8**

DESCRIPTION:

This specification sheet details the K&M bipolar current source (K&M part number 2494). The supply is a voltage controlled - current source that supplies the needle current in the APCI accessory of the Sprite (G1946A) Ion Source.

Physical:

Refer to D-G1946-80014-1 PHYSICAL DRAWING for details on the mechanical specification as well as the I/O ribbon cable pin out.

Electrical Input:

Voltage:	24 VDC +/-2V	
Current:	800mA	Max

Current Output:

Voltage:	+/-(0.3 - 5)KVDC	Min/Max
Current (POS)[1]:	0.1 to 10uADC	Max
Current (NEG):	1.0 to 100uADC	Max
Ripple and Noise Voltage[2]:	1 Vp-p	Max

Stability:

Temperature Regulation:	250ppm of Vo/C	Max

Control Lines:

Shutdown Line:	High or Open = Supply OFF	Digital Input
Current control:	0 - 10VDC[3]	
Current control input impedance:	10 Kohm +/-0.1 Kohm	
Output Polarity:	TTL input[4]	

Monitor Lines:

Positive Status[5]:	Low = Positive output	Open Collector Output
Negative Status[6]:	Low = Negative output	Open Collector Output
Fault:	Low = Output fault	
Current Monitor Ratio:	1V/uA +/-(3%+50mV)	Positive Current
	-0.1V/uA +/-(3%+50mV)	Negative Current
Output voltage Monitor:	$V_{mon}=V_o/1000$ +/-(1%+5mV)	
Monitor Input Impedance	10 Kohm +/-0.1Kohm	

Reference Voltage:

Output Voltage	10VDC +/-1%

Electrical Safety:

LV RTN to HV RTN Isolation:	100 ohms || 0.1 uF	Nominal
HV RTN to Case Isolation:	shorted	

Environmental:

Operating Temperature:	-5C to 60C	Min to Max
Storage Temperature:	-40C to 70C	Min to Max
Operating Altitude:	15000/-1000 feet	Max/Min
Storage Altitude:	50000/-1000 feet	Max/Min
Humidity, Operating:	5 to 95%, non-condensing	Min to Max
Humidity, Non-operating	95%, 65C non-condensing	Max

Reliability:

Output is short circuit and arc protected.

Notes:

Note 1: The current output is different depending on the polarity of the output. When the output is Negative (this corresponds to Negative Ion Mode for the instrument), the output can handle 100uA. When the output is Positive, the output can handle 10uA. The factor of 10 difference is needed to support the APCI accessory in Negative Ion mode.

Note 2: Ripple and Noise Voltage is defined to include the following three catagories:

Broadband Random Noise
Random, non-switch related noise on the high voltage output.

Broadband Switching Noise:
Noise related to the oscillator, switching and feedback control circuitry other than ripple.

Ripple Noise:
Noise associated with the rectified primary switching frequency.

Note 3: V(ctl) is the control voltage.I(out) = V(ctl) * 1uA +/-(2%+50nA) for POS output.
I(out) = V(ctl) * -10uA +/-(2%+500nA) for NEG output.

Note 4: Polarity input is low for negative output. Polarity input high or floating will give a positive output.

Note 5: The Positive Status output is an open collector output meant to drive an LED to give a visual indication of whether the output is positive. A current limiting resistor is required.

Note 6: The Negative Status output is an open collector output meant to drive an LED to give a visual indication of whether the output is negative. A current limiting resistor is required.

E. Aisawa DRAWN BY	10/13/97	**+/-5KV HIGH VOLTAGE CURRENT SOURCE SPECIFICATION** TITLE	HEWLETT PACKARD
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E. Aisawa DRAWN BY	10/13/97	**+/-7KV DUAL OUTPUT HIGH VOLTAGE SUPPLY SPECIFICATION** TITLE	HEWLETT PACKARD
E. Aisawa ENGINEER	10/13/97		
N. Moreyra RELEASE TO PROD.	10/13/97		G1946-80015 PART NUMBER
SUPERSEDES DWG.	CURRENT REV A	PAGE 1 OF 4	**A-G1946-80015-8**

DESCRIPTION:

This specification sheet details the K&M bipolar high voltage module (K&M part number 2488F). This supply is a voltage controlled voltage output supply. The purpose of this supply is to supply voltage to two zones of the Sprite (G1946A) Ion Source.

Physical:

Refer to D-G1946-80015-1 PHYSICAL DRAWING for details on the mechanical specification as well as the I/O ribbon cable pin out.

Electrical Input:

Voltage:	24 VDC +/-10%	
Current:	800mA	Max

V1 Output -- Connectronics 15KV SCID Connector:

Voltage:	+/-(2 - 7)KVDC	Min/Max
Current:	0 to 2uADC	Max
Ripple and Noise Voltage[1]:	1 Vp-p	Max

V2 Output -- Connectronics 12KV MIDGI Connector:

Voltage:	+/-(1.5 - 6.5)KVDC[2]	Min/Max
Current (POS/NEG):	0 to 100uA/10uA[3]	
Ripple and Noise Voltage[1]:	1 Vp-p	Max

Regulation and Stability:

Line Regulation:	.1%	Max
Load Regulation:	.1%	Max
Temperature Regulation:	200ppm of Vo/C	Max

Control Lines:

Shutdown Line:	High or Open = Supply OFF	Digital Input
V1 control:	0 - 7VDC[4]	
Control Loop Input Impedance:	100 Kohm	Minimum
Output Polarity:	TTL input[5]	
nAPCI input:	TTL input[6]	

Monitor Lines:

Positive Status[7]:	Low = Positive output	Open Collector Output
Negative Status[8]:	Low = Negative output	Open Collector Output
Fault:	Low = Output fault	
HV Monitor Ratio[9]:	1000:1 +/-(0.75% + 25mV)	
V1 Current Monitor:	5V/uA +/-5%	
V2 Current Monitor:	1V/uA +/-(5%+60mV)	All modes except
V2 Current Monitor:	0.1V/uA+/-(5%+60mV)	Polarity is POS and nAPCI

		is low

Reference Voltage:

Output Voltage	10VDC	typical
Reference Output Impedance	10 Kohm	Max

Electrical Safety:

LV RTN to HV RTN Isolation:	100 ohms || .1 uF	Nominal
HV RTN to Case Isolation:	shorted	

Environmental:

Operating Temperature:	-5C to 60C	Min to Max
Storage Temperature:	-40C to 70C	Min to Max
Operating Altitude:	15000/-1000 feet	Max/Min
Storage Altitude:	50000/-1000 feet	Max/Min
Humidity, Operating:	5 to 95%, non-condensing	Min to Max
Humidity, Non-operating	95%, 65C non-condensing	Max

Reliability:

HED output is short circuit and arc protected.

Notes:

Note 1: Ripple and Noise Voltage is defined to include the following three catagories:

Broadband Random Noise
Random, non-switch related noise on the high voltage output.

Broadband Switching Noise:
Noise related to the oscillator, switching and feedback control circuitry other than ripple.

Ripple Noise:
Noise associated with the rectified primary switching frequency.

Note 2: The V2 output tracks the V1 output with a 500V offset. V2 is always 500V closer to 0V than

V1 (e.g. V1=5000V -> V2=4500V, V1=-5000V -> V2=-4500V). There is a tolerance of +/-20V on the 500V offset.

Note 3: The current output of the V1 output is different depending on the polarity of the output. When the output is Positive (this corresponds to Negative Ion Mode for the instrument), the output can handle 100uA. When the output is Negative, the output can handle 10uA. The factor of 10 difference is needed to support the APCI accessory in Negative Ion mode.

Note 4: V1(ctl) is the control voltage. V1(out) = V1(ctl) * 1000 +/-(0.75%+25V). V2 is slaved to V1.

Note 5: Polarity input is low for negative output. Polarity input high or floating will give a positive output.

Note 6: The nAPCI pin is used to inform the supply when the instrument is in APCI mode. A low on this input indicates that the APCI spray chamber is installed. APCI operation requires a factor of 10 greater current, in Negative Ion mode, than standard Electrospray. The supply uses this signal, along with the polarity input, to change the current output capability of the V2 output from 10 to 100 microamps. This supply is positive in Negative Ion mode.

Note 7: The Positive Status output is an open collector output meant to drive an LED to give a visual indication of whether the output is positive. A current limiting resistor is required.

Note 8: The Negative Status output is an open collector output meant to drive an LED to give a visual indication of whether the output is negative. A current limiting resistor is required.

Note 9: The output voltage monitor pin can be either monitoring the V1 or V2 ouput. The monitored output is set by the positions of two rocker switches. This is shown on the mechanical drawing for the supply (D-G1946-80015-1). The default is to monitor the V1 output.

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E. Aisawa DRAWN BY	10/13/97	**10KV BIPOLAR SUPPLY SPECIFICATION DRAWING** TITLE	HEWLETT PACKARD
E. Aisawa ENGINEER	10/13/97		
N. Moreyra RELEASE TO PROD.	10/13/97		G1946-80029 PART NUMBER
SUPERSEDES DWG.	CURRENT REV A	PAGE 1 OF 5	**A-G1946-80029-8**

DESCRIPTION:

This specification sheet details the K&M bipolar high voltage module (K&M part number 2496). This is a fixed bipolar 10KV supply. There is a provision, however, to change the output voltage (see Note 8). This is typically used only during test.

Physical:

Refer to D-G1946-80029-1 PHYSICAL DRAWING for details on the mechanical specification as well as the I/O ribbon cable pin out.

Electrical Input (Note 1):

Voltage:	24 +/- 2 VDC	Max/Min
Current:	300 mADC	Max
Ripple Current:	30 mAp-p	Max

HED Output -- Connectronics Connector (Note 2):

Voltage:	+/-10 KVDC +/- 100 VDC	Max/Min
Current:	0 to 10 uADC	Meeting all specifications
Ripple and Noise Voltage (Note 3):	500 mVp-p	Max
Oscillator 1 Frequency (Negative):	51 KHz +/-10%	Max/Min
Oscillator 2 Frequency (Positive):	64 KHz +/-10%	Max/Min

High Voltage Return -- Molex plug on flying lead (Note 4):

Regulation and Stability:

Line Regulation:	.1% of HED Vo	Max
Load Regulation:	.1% of HED Vo	Max
Temperature Regulation:	300ppm of HED Vo/C	Max
Short Term Stability (Note 5):	.1% of HED Vo per hour	Max
Long Term Stability(Note 6):	.5% of HED Vo per year	Max

Control Lines:

Enable Line (Note 7):	High or Open = HED OFF	Digital Input
Polarity Selection:	High or Open = Positive Pol	Digital Input
Control Loop Input (Note 8):	0 to 8 VDC	Min to Max
Control Loop Input Impedance:	10 Kohm	Minimum

Monitor Lines:

Status Line (Note 9):	Low = Fault	Digital Output
HV Monitor Line (Note 10):	3333 (+/-1%) : 1	Max/Min Ratio
Internal Reference Output (Note 11):	5 VDC +/- .025 VDC	Max/Min
Reference Output Impedance	10 Kohm +/- 1 Kohm	Max/Min

Electrical Safety:

HED Decay Time (Note 12):	5 seconds	Max
LV RTN to HV RTN Isolation:	100 ohms || .47 uF	Nominal
LV RTN to Case Isolation:	100 ohms || .47 uF	Nominal

Environmental

Operating Temperature:	-5C to 60C	Min to Max
Storage Temperature:	-40C to 70C	Min to Max
Operating Altitude:	15000/-1000 feet	Max/Min
Storage Altitude:	50000/-1000 feet	Max/Min
Humidity, Operating:	5 to 95%, non-condensing	Min to Max
Humidity, Non-operating	95%, 65C non-condensing	Max

Reliability:

HED output is short circuit and arc protected.

Notes:

Note 1: The standard test configuration is as follows:

Enable Line:	Low
Control loop input terminal	Open
HED output	1 uADC load
DIF output	500 nADC load
+24VDC In	+24VDC
LV commons	All tied to +24V rtn
HV common	Open
Case	Floating
Ambient Temperature:	23 C

Note 2: HED stands for High Energy Dynode. HED output voltage is measured using the standard test configuration specified in Note 1.

Note 3: Ripple and Noise Voltage is defined to include the following three catagories:

Broadband Random Noise
Random, non-switch related noise on the high voltage output.

Broadband Switching Noise:
Noise related to the oscillator, switching and feedback control circuitry other than ripple.

Ripple Noise:
Noise associated with the rectified primary switching frequency.

Note 4: The High Voltage return is a green wire on pin 2 of the Molex Minifit Jr plug. Its intended use is to return energy generated from an arc back to the supply.

Note 5: Stability is specified using the standard test configuration specified in Note 1, however temperature is a varied through the specified operating range. Stability is specified with constant temperature after a one hour warm-up.

Note 6: Long term stability is additive to the initial voltage accuracy spec. For example, a new module's HED output must be +/-100 VDC as received by HP but when this module is 1 year old, it need only be +/-150 VDC to be considered acceptable. Considering a 10 year life for the instrument, the HED output could be as much as 600V from nominal. Should the HED output drift low by that amount, the customer may begin to notice a very slight degradation in high mass abundance.

Note 7: Guaranteed enable is .5 VDC or less while guaranteed disable is 1.5 VDC or more. The Rthevinen = 3.3 Kohm (typical) while the Vthevinen = 8.5 VDC (typical).

Note 8: For normal (+/-10 KVDC output) operation, the Control Loop Input Terminal is open. The output voltage can be varied between 2.5 KVDC and 10 KVDC by a voltage applied to the Control Loop Input terminal according to the formula:

| HV Output | = 2500V + Control Loop Input Terminal Voltage * (937.5 +/- 3%)

Note 9: In a fault situation, this output is guaranteed to be 1.1 VDC or less. While in fault, the Rthevinen = 160 ohms (typical) while the Vthevinen = 0 VDC (typical). While not in fault, the Rthevinen = 2.7 Kohms (typical) while the Vthevinen = 4.3 VDC (typical).

Note 10: The HV Monitor Line is referenced to the Internal Reference Output and has an Rthevinen of 10Kohms. The HV Monitor output is negative with respect to the Reference Output. With the Control Loop Input terminal open, the HV Monitor Line has an output of 2V while the Control Loop Input terminal is at 5V.

3333 * (2 - 5) = -10KV

Note 11: The Internal Reference Output meets listed specifications when the Control Loop Input terminal is open. When the Control Loop Input terminal voltage is varied, the Reference Output voltage varies according to the following formula:

Reference Output = 1.25V + Control Loop Input Terminal Voltage * (.469 +/- 3%)

Note 12: The HV output shall decay to less than -60V within the specified time whenever the input power is removed or the supply is disabled.

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N. Moreyra RELEASE TO PROD.	10/13/97		G1946-80029 PART NUMBER
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E. Aisawa DRAWN BY	10/13/97	**Sprite Turbo Power Supply Specification** TITLE	HEWLETT PACKARD
E. Aisawa ENGINEER	10/13/97		
N. Moreyra RELEASE TO PROD.	10/13/97		G1946-80032 PART NUMBER
SUPERSEDES DWG.	CURRENT REV A	PAGE 1 OF 12	**A-G1946-80032-8**

Hewlett-Packard Turbo Controller
Power Supply Specification
G1946-80032

This specification defines a 200 watt power supply. The power supply will have a wide range AC front end operating from a single phase 200/220/240 volts nominal source. The output will feed a box which will interface with two Edwards EXDC type Drive Cards. This box will supply power and control logic to the Drive Cards. The intended application for the supply is to supply power to two EXDC turbo controllers for a differentially pumped vacuum system. The vacuum system is part of a mass spectrometer used in laboratory and industrial environments.

1.0 Regulatory Requirements

1.1 Safety

1.1.1 The power supply must be compliant to and certified by Underwriters Laboratories (UL) as compliant with specification UL 1950 and applicable portions of UL 3101-1

1.1.2 The power supply must be compliant to the International Electrotechnical Commission (IEC), IEC 1010-1

1.1.3 The power supply must be compliant to the European Community for Electrotechnical Standardization (CENELEC), EN 61010-1

1.1.4 The power supply must be compliant to, certified by the Canadian Standards Association (CSA) or a recognized NRTL as compliant with, and labelled indicating compliance to; CAN/CSA C22.2 No. 234 level 3 (CSA certification)

1.1.5 In the event of loss of main power, the supply must drop below 60VDC in 0.2 seconds and be below 5 volts in 5 seconds. This test is performed with no load on the output. The supply must also tolerate the back emf generated by the EXDC controllers when the turbos are turned off.

1.2 Electromagnetic Interference

1.2.1 The power supply must be compliant to CISPR 11, conducted emissions Class B with 6 dB of margin (average criteria)

1.2.2 The power supply must be compliant to CISPR 11, radiated emissions Class B with 6 dB of margin (full resistive load on the end of a 1 meter cable)

1.2.3 The power supply must be compliant to IEC 801-4 level 3

1.2.4 The power supply must be compliant to the Institute of Electrical and Electronic Enginneers (IEEE)/American National Standards Institute (ANSI), ANSI/IEEE C62.41 (Installation Category B2)

2.0 Input Electrical Requirements

2.1 Electrical Parameters

Table 1: Electrical Parameters

Parameter	Range	Condition
2.1.1 Input Voltage	180 to 264 VAC RMS	Wide range input required without user action. Range will be tested 176 - 269 VAC RMS.
2.1.2 Input Frequency	47 to 63 Hertz	
2.1.3 Inrush Current	Less than 20 A peak, Peak shall last no more than one full line cycle.	Over entire input frequency range.
2.1.4 Input Fusing	Whatever is appropriate	Entire Operating Conditions
2.1.5 Efficiency	Greater than 70%	At max load, input voltage 180 VAC; 47 Hertz.
2.1.6 Power Factor	Greater than 95%	At max load. Over full voltage range of the supply.
2.1.7 Leakage Current	Less than 1 mA	At full load; input voltage 264 VAC RMS; 66 Hertz.
2.1.8 Hi-Pot	Using a 2121 VDC potential and tying the two primary conductors together, there shall be no dielectric breakdown or failure between either primary terminal and the safety ground.	

Table 1: Electrical Parameters

Parameter	Range	Condition
2.1.9 Line Transients	a. Low Energy Pulse - 100 KHz “ring wave” with 4 KV amplitude into an open circuit per ANSI/IEEE C62.41	Over the complete power supply range. power supply must continue to function and meet all specifications.
	b. Low Energy Pulse - 100 KHz “ring wave” with 6KV amplitude into an open circuit per ANSI/IEEE C62.41	Over the complete power supply range. Supply must continue to function. A reset is allowed here.
	c. High Energy Pulse - 1000 Volt Pulse of 1. 2 us rise time decaying to 500V in 50 us. into an open circuit per ANSI/IEEE C62.41	Over the complete power supply range. Supply must continue to function and meet all specifications.
2.1.10 Hold Up Time	One full zero crossing line cycle.	Full rated load at 180 VAC RMS; 47 Hertz
2.1.11 Total Harmonic Distortion	Maximum of 5%	At max load.
2.1.12 Transparent Surge	Step from 264V to 293V for 500 ms.	Complete power load of supply. Outputs should remain functional and within specifications during this test.
2.1.13 Line Surge	Step from 259V to 300V for 500 ms and return to 259V.	Complete power load of supply. No permanent damage may occur. An open fuse is considered a failure.
2.1.14 Line Sag	Step from 180V to 135V for 500 ms and return to 180V.	Complete power load of supply. No permanent damage may occur. An open fuse is considered a failure.

Table 1: Electrical Parameters

Parameter	Range	Condition
2.1.15 Line Brownout and Recovery	a. Linearly decrease from 180V to 0V in 30 minutes. Then reapply 180V. b. Linearly increase input voltage from 0 to 180V in 30 minutes.	Power supply at full load; line frequency at 60 Hz. Supply must return to normal operation. Open fuse is a failure. Same as above.
2.1.16 Line Dropout	Step from 180V to 0V for 20 ms. Then reapply 180V.	Dropout is initiated at the zero-crossing of the sine wave. Dropout should be transparent. Supply should remain functional and within specs during this test.

3.0 Output Electrical Requirements

Table 2: Power Supply Output Requirements

Parameter	Range	Condition
3.0.1 Output Nominal (Volts - DC)-	75 volts	no minimum load
3.0.2 Output LED		LED is on when output voltage present
3.0.3 Output Current (Amperes)	0-3 amps	
3.0.4 Line Regulation	Note 1	max load; low line to high line
3.0.5 Load Regulation	Note 1	
3.0.6 Ripple and Noise	10 V p-p maximum	minimum input line and frequency; full output load. Also, see Note 1
3.0.7 Transient Response	Recovery 1 ms max to within 1% Vout	50-100% load
3.0.8 Overvoltage Protection	120% of max	Any condition
3.0.9 Overcurrent Protection	3.3 amps typical	
3.0.10 Temperature Coefficient	Note 1	Entire temperature range

Note 1: Output may not be outside the range of 70 - 85 volts DC (including ripple).

4.0 Environmental

4.1 Operating Temperature

-5 to 60 degrees Celsius between pressure altitudes of -1000 feet to 7500 feet

Linearly derated above 7500 feet by 1.1 degrees C / 1000 feet

4.2 Survival Temperature:

Operating: -5 to 60 degrees Celsius

Non-operating: -40 degrees to 70 degrees Celsius

4.3 Operating Humidity

5% to 95% non-condensing at 40 degrees Celsius

4.4 Non-Operating Humidity

The power supply shall be subjected to 90% relative humidity for a period of twenty-four hours at 65 degrees Celsius. At the end of this period the power supply shall not have suffered any permanent damage. Further, the power supply shall have no mold, rust, or other consequential defects.

4.5 Altitude

4.5.1 Operating Altitude: -1000 to 15000 feet

4.5.2 Survival Altitude: -1000 to 50000 feet

4.6 Operation Vibration

The power supply must meet all specification during the test with power on, full load. The test consist of random vibration, with the following power spectral density, for ten minutes per axis; on each of the three axes.

Table 3: Operation Vibration Conditions

Frequency	Power Spectral Density	Slope
4.6.1 5 to 350 Hz	0.0001 g^2 per Hz	0 db/octave
4.6.2 350 to 500 Hz		-6 db/octave
4.6.3 500 Hz	0.00005 g^2 per Hz	0 db/octave

4.7 Survival Vibration

4.7.1 Random Vibration

The power supply shall withstand the following random vibration for ten minutes per axis, on all three axes, without sustaining permanent damage.

Table 4: Random Vibration Conditions

Frequency	Power Spectral Density	Slope
4.7.2 5 to 100Hz	0.015 g^2 per Hz	0 db/octave
4.7.3 100 to 137 Hz		-6 db/octave
4.7.4 137 to 350 Hz	0.0080 g^2 per Hz	0 db/octave
4.7.5 350 to 500 Hz		-6 db/octave
4.7.6 500 Hz	0.0039 g^2 per Hz	0 db/octave

4.7.7 Swept Sine

The power supply shall survive without permanent damage being subjected to a sine wave of 0.5G, zero to peak, from 5 to 500 Hertz, at a rate of one octave per minute. The four largest amplitude resonating frequencies shall be noted and the power supply subject to five minutes at each of these frequencies. This test shall be repeated for each axis.

4.8 Radiated Susceptibility

The power supply shall meet all specifications when subject to a radiated field of 10 volts per meter over the frequency range of 14 Kilohertz to 1000 Megahertz.

4.9 Conducted Susceptibility

The power supply shall meet all specifications when subject to three volts rms over the frequency range of 30 Hz to 50 KHz applied to the supply's power leads.

The power supply shall meet all specifications when subject to one volt rms over the frequency range fo 50 KHz to 400 MHz applied to the supply's power leads.

4.10 Magnetic Susceptibility

The power supply shall continue to operate, meeting all specifications, in a uniform field of 0.1 millitesla (1 gauss) peak-to-peak over a freqency range of 47.5 to 198 Hz. The power supply shall continue to operate in specification with the magnetic fields applied in any orientation with respect to the supply.

4.11 Magnetic Interference

4.11.1 Operating

The power supply shall not emit a magnetic field greater than 0.1 millitesla (1 gauss) peak-to-peak from DC to 400 Hz.

4.11.2 Non-Operating

The power supply, not operating, shall not emit a magnetic field greater than 1.5 milligauss at a distance of 7 feet from any surface of the supply.

5.0 Mechanical Requirements

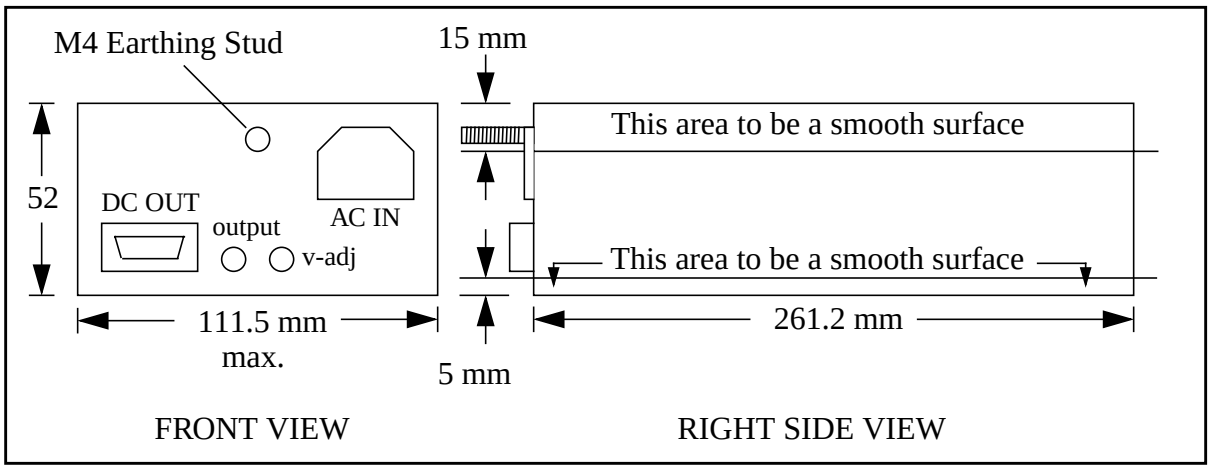
5.1 Packaging

The power supply packaging shall have a maximum external dimension of 261.2 mm (L), 52.0 mm (H), and 115.5 mm (W). The AC input connector and output connector shall be placed on the same 115 x 52 face of the package along with an M4 earthing stud.

The packaging shall be protected by an electrically conductive coating. There should be <0.1 ohms between any two points on the package.

The top, bottom, and left side of the supply must remain flush with the sheet metal. Pan head screws may be used on the right side as long as the contribution to the width does not exceed the 115.5 mm maximum and they are not located in the keep out area of the right side (shown in the drawing below).

There shall be a 15 mm minimum clearance along the top of each side that runs the length of the supply that must remain flush with the sheet metal. Also, there is a 5 mm minumum clearance that runs along the bottom of each side that runs the length of the supply that also must remain flush with the sheet metal.



5.2 Connectors

5.2.1 Input Line Connector

The input AC receptacle shall be of the type described by IEC 320 standard sheet C14

5.2.2 Output Connector

The output connector shall be a Female DB-9 connector whose metal shell is electrically connected to the supply's outer packaging. The pin assignments are listed in the following table:

Table 5: Power Supply Output Pin Assignments

Pin #	Name
1	+75V Ret
2	+75V Ret
3	+75V
4	+75V
5	CH GND
6	+75V Ret
7	+75V Ret
8	+75V
9	+75V

5.3 Cooling

The instrument will provide 2 liter/sec air flow over the supply. The supply will provide its own overtemperature protection in the event of insufficient cooling so that there is no component damage. The supply will come back on line when the temperature falls back into its safe operating range.

6.0 Labels and Markings

6.1 Regulatory Requirements

The power supply shall be labelled with all regulatory stamps or seals the assembly has met certification for.

6.2 Nameplate Information

The power supply shall have the following information, labelled in English, affixed in a visible area.

Hewlett Packard Part Number

Serial Number

Manufacturer Part Number and Latest Revision

Manufacturer Company Name

Nominal Input Voltages and Frequencies

Nominal Output voltages and Rated Currents

HEWLETT-PACKARD
California Analytical Division
1601 California Avenue
Palo Alto, California 94304

REV	REVISIONS	APPROVED	DATE
A	AS ISSUED PER PC23-6030	N. Moreyra	10/13/97
B	Changed input specification from 180-264VAC to 85-264VAC per EC23-70145	M. Lam	09/28/98

Hewlett-Packard
Power Supply Specification
G1946-80037

This specification defines a 365 watt (DC) switching power supply with a wide range AC front end operating from a single phase 200/220/240 volts nominal source. This supply will also have an additional output connector to supply primary power to an 800 VA transformer. The intended application for the power supply is a mass spectrometer used in laboratory and industrial environments.

1.0 Regulatory Requirements

1.1 Safety

1.1.1 The supply must be compliant to and certified by Underwriters Laboratories (UL) or a Nationally Recognized Test Lab (NRTL) as compliant with specification UL 1950 and applicable portions of UL 3101-1

1.1.2 The supply must be compliant to the International Electrotechnical Commission (IEC), IEC 1010-1

1.1.3 The supply must be compliant to the European Community for Electrotechnical Standardization (CENELEC), EN 61010-1

1.1.4 The supply must be compliant to, certified by the Canadian Standards Association (CSA) or an NRTL as compliant with, and labelled indicating compliance to; CAN/CSA C22.2 No. 234 level 3 (CSA certification)

1.2 Electromagnetic Interference

1.2.1 The supply must be compliant to CISPR 11, conducted emissions Class B with 6 dB of margin

1.2.2 The supply must be compliant to IEC 801-4 level 3

1.2.3 The supply must be compliant to the Institute of Electrical and Electronic Enginneers (IEEE)/ American National Standards Institute (ANSI), ANSI/IEEE C62.41 (Installation Category B2)

2.0 Input Electrical Requirements

2.1 Electrical Parameters

Table 1: Electrical Parameters

Parameter	Range	Condition
2.1.1 Input Voltage	85 to 264 VAC RMS	Wide range input required without user action. Range will be tested 176 - 269 VAC RMS.
2.1.2 Input Frequency	47 to 63 Hertz	
2.1.3 Inrush Current	Less than 20 A peak, Peak shall last no more than one full line cycle.	Over entire input frequency range.
2.1.4 Input Fusing	Externally fused at 6 A.	
2.1.5 Efficiency	Greater than 70%	At max load, input voltage 180 VAC; 47 Hertz.
2.1.6 Power Factor	Greater than 95%	At max load. Over full voltage range of the supply.
2.1.7 Leakage Current	Less than 2 mA	At full load; input voltage 264 VAC RMS; 66 Hertz.
2.1.8 Hi-Pot	Using a 2121 VDC potential and tying the two primary conductors together, there shall be no dielectric breakdown or failure between either primary terminal and the safety ground.	

Table 1: Electrical Parameters

Parameter	Range	Condition
2.1.9 Line Transients	a. Low Energy Pulse - 100 KHz “ring wave” with 4 KV amplitude into an open circuit per ANSI/IEEE C62.41	Over the complete supply range. Supply must continue to function and meet all specifications.
	b. Low Energy Pulse - 100 KHz “ring wave” with 6KV amplitude into an open circuit per ANSI/IEEE C62.41	Over the complete supply range. Supply must continue to function. A reset is allowed here.
	c. High Energy Pulse - 1000 Volt Pulse of 1. 2 us rise time decaying to 500V in 50 us. into an open circuit per ANSI/ IEEE C62.41	Over the complete supply range. Supply must continue to function and meet all specifications.
2.1.10 Hold Up Time	One full zero crossing line cycle.	Full rated load at 180 VAC RMS; 47 Hertz
2.1.11 Total Harmonic Distortion	Maximum of 5%	At max load.
2.1.12 Transparent Surge	Step from 264V to 293V for 500 ms.	Complete power load of supply. Outputs should remain functional and within specifications during this test.
2.1.13 Line Surge	Step from 259V to 300V for 500 ms and return to 259V.	Complete power load of supply. No permanent damage may occur. An open fuse is considered a failure.
2.1.14 Line Sag	Step from 180V to 135V for 500 ms and return to 180V.	Complete power load of supply. No permanent damage may occur. An open fuse is considered a failure.

Table 1: Electrical Parameters

Parameter	Range	Condition
2.1.15 Line Brownout and Recovery	a. Linearly decrease from 180V to 0V in 30 minutes. Then reapply 180V.	Power supply at full load, line frequency at 60 Hz. Supply must return to normal operation. Open fuse is a failure.
	b. Linearly increase input voltage from 0 to 180V in 30 minutes.	Same as above.
2.1.16 Line Dropout	Step from 180V to 0V for 20 ms. Then reapply 180V.	Dropout is initiated at the zero-crossing of the sine wave. Dropout should be transparent. Supply should remain functional and within specs during this test.

3.0 Output Electrical Requirements

3.1 +5 Volt Output

Table 2: +5 Volt Requirements

Parameter	Range	Condition
3.1.1 Output Nominal (Volts - DC)-	4.95 to 5.2 volts	no minimum load
3.1.2 Output Current (Amperes)	1 to 10 amps	
3.1.3 Line Regulation	0.2% maximum	max load; low line to high line
3.1.4 Load Regulation	0.2% maximum	
3.1.5 Ripple and Noise	100 mV p-p maximum	minimum input line and frequency; full output load
3.1.6 Transient Response	Recovery 1 ms max to within 1% Vout	50-100% load
3.1.7 Overvoltage Protection	120%	Any condition
3.1.8 Overcurrent Protection	12 amps typical	
3.1.9 Temperature Coefficient	0.02% per degree C	Above and below 25 deg C.

3.2 +15 Volt Output

Table 3: +15 Volt Requirements

Parameter	Range	Condition
3.2.1 Output Nominal (Volts - DC)-	14.8 to 15.2 volts	no minimum load
3.2.2 Output Current (Amperes)	0 to 3 amps	
3.2.3 Line Regulation	0.1% maximum	max load; low line to high line
3.2.4 Load Regulation	0.5% maximum	
3.2.5 Ripple and Noise	100 mV p-p maximum	minimum input line and frequency; full output load
3.2.6 Transient Response	Recovery 1 ms max to within 1% Vout	50-100% load
3.2.7 Overvoltage Protection	120%	Any condition
3.2.8 Overcurrent Protection	5 amps typical	
3.2.9 Temperature Coefficient	0.06% per degree C	Above and below 25 deg C.

3.3 -15 Volt Output

Table 4: -15 Volt Requirements

Parameter	Range	Condition
3.3.1 Output Nominal (Volts - DC)-	-15.2 to -14.8 volts	no minimum load
3.3.2 Output Current (Amperes)	0 to 2 amps	
3.3.3 Line Regulation	0.1% maximum	max load; low line to high line
3.3.4 Load Regulation	0.5% maximum	
3.3.5 Ripple and Noise	100 mV p-p maximum	minimum input line and frequency; full output load
3.3.6 Transient Response	Recovery 1 ms max to within 1% Vout	50-100% load
3.3.7 Overvoltage Protection	120%	Any condition
3.3.8 Overcurrent Protection	5 amps typical	
3.3.9 Temperature Coefficient	0.06% per degree C	Above and below 25 deg C.

3.4 +24 Volt Output

Table 5: +24 Volt Requirements

Parameter	Range	Condition
3.4.1 Output Nominal (Volts - DC)-	23.75 to 24.25 volts	no minimum load
3.4.2 Output Current (Amperes)	1 to 4 amps	
3.4.3 Line Regulation	0.2% maximum	max load; low line to high line
3.4.4 Load Regulation	0.2% maximum	
3.4.5 Ripple and Noise	200 mV p-p maximum	minimum input line and frequency; full output load
3.4.6 Transient Response	Recovery 1 ms max to within 1% Vout	50-100% load
3.4.7 Overvoltage Protection	120%	Any condition
3.4.8 Overcurrent Protection	5.5 amps typical	
3.4.9 Temperature Coefficient	0.02% per degree C	Above and below 25 deg C.

3.5 +28 Volt Output

Table 6: +28 Volt Requirements

Parameter	Range	Condition
3.5.1 Output Nominal (Volts - DC)-	27.5 to 28.5 volts	no minimum load
3.5.2 Output Current (Amperes)	1 to 6 amps	
3.5.3 Line Regulation	0.2% maximum	max load; low line to high line
3.5.4 Load Regulation	0.2% maximum	
3.5.5 Ripple and Noise	500 mV p-p maximum	minimum input line and frequency; full output load
3.5.6 Transient Response	Recovery 1 ms max to within 1% Vout	50-100% load
3.5.7 Overvoltage Protection	120%	Any condition
3.5.8 Overcurrent Protection	7.2 amps typical	
3.5.9 Temperature Coefficient	0.06% per degree C	Above and below 25 deg C.

4.0 Control Signals

4.1 +5, +/-15 Remote ON/OFF

The supply shall provide a TTL-compatible input which, when grounded, will turn off the +5 and +/-15 volt supplies. The input shall not require an external pull-up.

4.2 +24 Remote ON/OFF

The supply shall provide a TTL-compatible input which, when grounded, will turn off the +24 volt supply. The input shall not require an external pull-up.

NOTE: By the topology of the power supply (two stacked 24V supplies to get 48 volts) turning off the +24V supply should also turn off the +48V supply.

4.3 +28 Remote ON/OFF

The supply shall provide a TTL-compatible input which, when grounded, will turn off the +28 volt supply. The input shall not require an external pull-up.

4.4 Output OK

The supply shall provide a TTL-compatible output (active low) which will indicate that the supply outputs are functional and within specifications.

5.0 Environmental

5.1 Operating Temperature

-5 to 60 degrees Celsius between pressure altitudes of -1000 feet to 7500 feet

Linearly derated above 7500 feet by 1.1 degrees C / 1000 feet

5.2 Survival Temperature:

Operating: -5 to 60 degrees Celsius

Non-operating: -40 degrees to 70 degrees Celsius

5.3 Operating Humidity

5% to 95% non-condensing at 40 degrees Celsius

5.4 Non-Operating Humidity

The supply shall be subjected to 90% relative humidity for a period of twenty-four hours at 65 degrees Celsius. At the end of this period the supply shall not have suffered any permanent damage. Further, the supply shall have no mold, rust, or other consequential defects.

5.5 Altitude

5.5.1 Operating Altitude: -1000 to 15000 feet

5.5.2 Survival Altitude: -1000 to 50000 feet

5.6 Operation Vibration

The power supply must meet all specification during the test with power on, full load. The test consist of random vibration, with the following power spectral density, for ten minutes per axis; on each of the three axes.

Table 7: Operation Vibration Conditions

Frequency	Power Spectral Density	Slope
5.6.1 5 to 350 Hz	0.0001 g^2 per Hz	0 db/octave
5.6.2 350 to 500 Hz		-6 db/octave
5.6.3 500 Hz	0.00005 g^2 per Hz	0 db/octave

5.7 Survival Vibration

5.7.1 Random Vibration

The power supply shall withstand the following random vibration for ten minutes per axis, on all three axes, without sustaining permanent damage.

Table 8: Random Vibration Conditions

Frequency	Power Spectral Density	Slope
5.7.2 5 to 100Hz	0.015 g^2 per Hz	0 db/octave
5.7.3 100 to 137 Hz		-6 db/octave
5.7.4 137 to 350 Hz	0.0080 g^2 per Hz	0 db/octave
5.7.5 350 to 500 Hz		-6 db/octave
5.7.6 500 Hz	0.0039 g^2 per Hz	0 db/octave

5.7.7 Swept Sine

The power supply shall survive without permanent damage being subjected to a sine wave of 0.5G, zero to peak, from 5 to 500 Hertz, at a rate of one octave per minute. The four largest amplitude resonating frequencies shall be noted and the supply subject to five minutes at each of these frequencies. This test shall be repeated for each axis.

5.8 Radiated Susceptibility

The supply shall meet all specifications when subject to a radiated field of 10 volts per meter over the frequency range of 14 Kilohertz to 1000 Megahertz.

5.9 Conducted Susceptibility

The supply shall meet all specifications when subject to three volts rms over the frequency range of 30 Hz to 50 KHz applied to the supply's power leads.

The supply shall meet all specifications when subject to one volt rms over the frequency range fo 50 KHz to 400 MHz applied to the supply's power leads.

5.10 Magnetic Susceptibility

The power supply shall continue to operate, meeting all specifications, in a uniform field of 0.1 millitesla (1 gauss) peak-to-peak over a freqency range of 47.5 to 198 Hz. The supply shall continue to operate in specification with the magnetic fields applied in any orientation with respect to the power supply.

5.11 Magnetic Interference

5.11.1 Operating

The power supply shall not emit a magnetic field greater than 0.1 millitesla (1 gauss) peak-to-peak from DC to 400 Hz.

5.11.2 Non-Operating

The power supply, not operating, shall not emit a magnetic field greater than 1.5 milligauss at a distance of 7 feet from any surface of the supply.

6.0 Mechanical Requirements

6.1 Packaging

The supply packaging shall have an external dimension of 380 mm (L), 144 mm (H), and 80 mm (W).

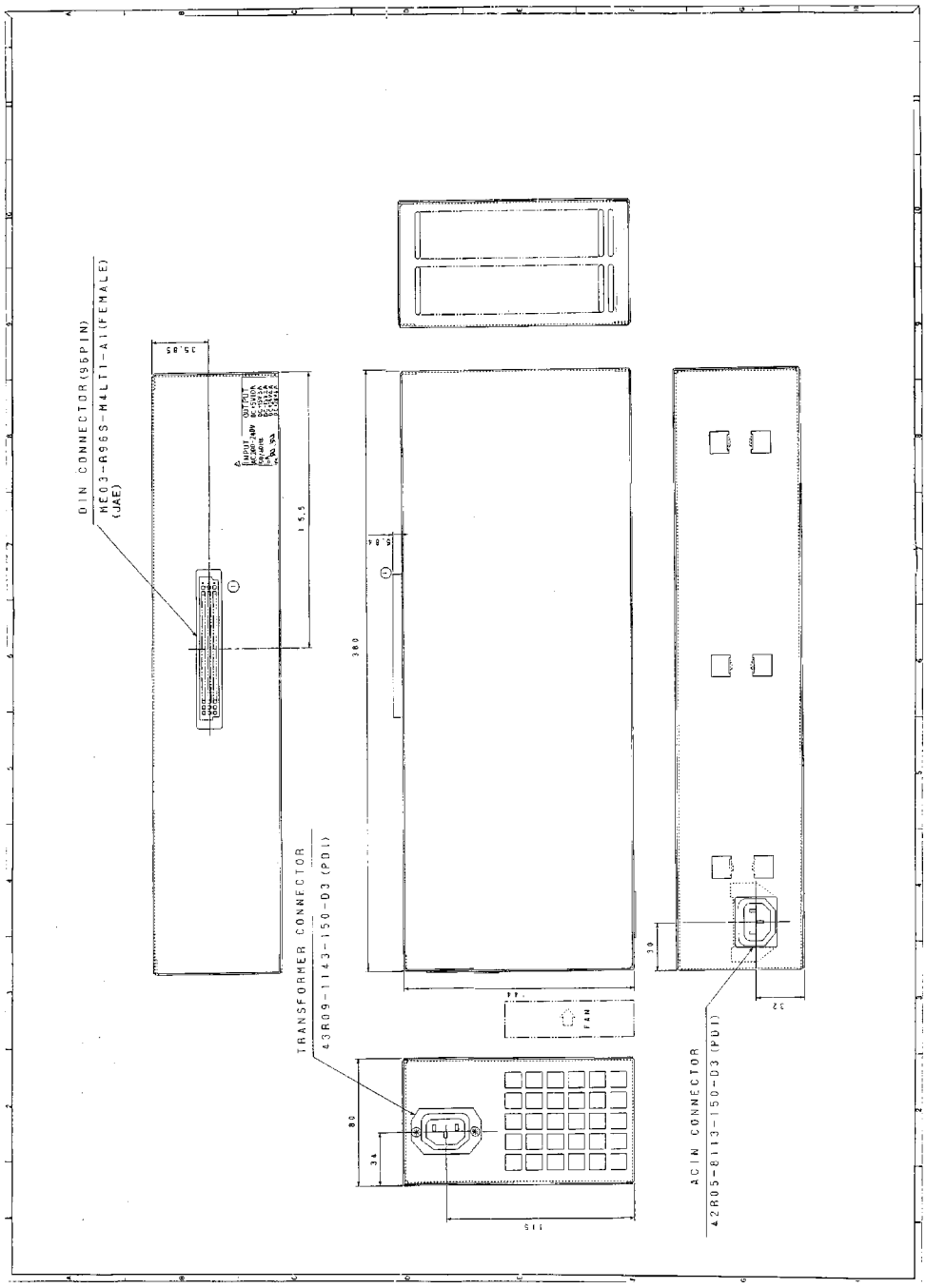


Figure 1: External Dimensions and Connector Locations

E. Aisawa DRAWN BY	10/13/97	**Sprite Main Power Supply Specification** TITLE	HEWLETT PACKARD
E. Aisawa ENGINEER	10/13/97		
N. Moreyra RELEASE TO PROD.	10/13/97		G1946-80037 PART NUMBER
SUPERSEDES DWG.	CURRENT REV B	PAGE 14 OF 17	**A-G1946-80037-8**

6.2 Connectors

6.2.1 Input Line Connector

The input AC receptacle shall be of the type described by IEC 320 standard sheet C13

6.2.2 DC Voltage Output Connector

The DC Voltage Connector shall be a 96 pin DIN connector (F). The pin assignments for a right angle 96 pin DIN Female connector is given in Table 9:

Table 9: Power Supply Output Pin Assignments[3]

	A	B	C
1	+/-15V RET	+/-15V RET	+/-15V RET
2	+/-15V RET	+/-15V RET	+/-15V RET
3	+5 RET	+5 RET	+5 RET
4	+5 RET	+5 RET	+5 RET
5	+5 RET	+5 RET	+5 RET
6[1]	+5 SENS-	+5 SENS-	+5 SENS-
7	-15V OUT	-15V OUT	-15V OUT
8	N/C	N/C	N/C
9	+15V OUT	+15V OUT	+15V OUT
10[1]	+5 SENS+	+5 SENS+	+5 SENS+
11	+5V OUT	+5V OUT	+5V OUT
12	+5V OUT	+5V OUT	+5V OUT
13	+5V OUT	+5V OUT	+5V OUT
14	+28V SENS+	+28V SENS+	+28V SENS+
15	+28V OUT	+28V OUT	+28V OUT
16	+28V OUT	+28V OUT	+28V OUT
17	+24V OUT	+24V OUT	+24V OUT
18	+24V OUT	+24V OUT	+24V OUT
19	+5,+/-15V ENABLE	+5,+/-15V ENABLE	+5,+/-15V ENABLE
20	+24V ENABLE	+24V ENABLE	+24V ENABLE

Table 9: Power Supply Output Pin Assignments[3]

	A	B	C
21	N/C	N/C	N/C
22	+28V ENABLE	+28V ENABLE	+28V ENABLE
23	N/C	N/C	N/C
24	OUTPUT OK	OUTPUT OK	OUTPUT OK
25	N/C	N/C	N/C
26[1]	+28V SENS-	+28V SENS-	+28V SENS-
27	+28V RET	+28V RET	+28V RET
28	+28V RET	+28V RET	+28V RET
29[2]	SG	SG	SG
30	+24V RET	+24V RET	+24V RET
31	+24V RET	+24V RET	+24V RET
32	+24V RET	+24V RET	+24V RET

Note 1: Sense Lines are internally connected to their respective supplies via a 10 ohm resistor. This is only present as a protection feature. The user is still expected to terminate these lines properly.

Note 2: SG is a signal ground pin and is the ground reference for the ENABLE inputs to the supply. It is also internally connected to the +24V RET lines.

Note 3: Extreme care should be taken when looking at row numbers on DIN connectors. Row numbers match up when a right angle connector is mated with a vertical mount connector. Row numbers are turned around, however, when either a right angle connector is mated to another right angle connector or when a vertical mount connector is mated with another vertical mount connector. Table 9 lists the signal names by the row number as labelled on the connector. The vendor's schematic has turned the row numbers around. To match Table 9 to the vendor's schematic, reverse the row numbers (e.g. row 1 is row 32 on the schematic, row 2 is row 31 on the schematic, etc.).

6.2.3 Transformer Primary Power Connector

The power connector for the transformer shall be a "Reverse" IEC 320 connector.

6.3 Cooling

Air will be supplied to the power supply from the end product. The airflow supplied to the power supply will come on the side of the supply at a rate of twenty-five cubic feet per minute. The air temperature will be approximately 5 degrees Celsius above ambient.

7.0 Labels and Markings

7.1 Regulatory Requirements

The power supply shall be labelled with all regulatory stamps or seals the assembly has met certification for.

7.2 Nameplate Information

The power supply shall have the following information, labelled in English, affixed in a visible area.

Hewlett Packard Part Number

Serial Number

Manufacturer Part Number and Latest Revision

Manufacturer Company Name

Nominal Input Voltages and Frequencies

Nominal Output voltages and Rated Currents

HEWLETT-PACKARD
California Analytical Division
1601 California Avenue
Palo Alto, California 94304

REV	REVISIONS	APPROVED	DATE
A	Released from Rev 1 w/ changes per EC23-70263	K. Horstman	04/08/99

M. Lam DRAWN BY	04/24/98	**40 uA (±5.5 kV Compliant) Fast-Reversing Current Source Specification** TITLE	HEWLETT PACKARD
B. Crawford ENGINEER	04/24/98		
K. Horstman RELEASE TO PROD.	04/08/99		G1946-80058 PART NUMBER
SUPERSEDES DWG.	CURRENT REV A	PAGE 1 OF 4	**A-G1946-80058-2**

Description:

This specification sheet details the fast-reversing current source. It is a voltage-controlled current source with a compliance voltage up to ±5.5 kV. Its purpose is to control the needle current in the APCI accessory to the LC/MS Ion Source.

Input Control: Voltage controlled **Output Type:** Current source, variable
Number of outputs: 1 output: (1) 40 uA, up to ±5.5 kV for compliance

Electrical Input:

Voltage:	$24 \pm 2\ V_{DC}$
Current:	$\leq 400\ mA_{DC}$
Ripple Current:	$\leq 30\ mA_{P-P}$

I1 Output:

Load Conditions:

System Load:	20 pF (source) + 10 pF (cable) + output current
Bench Test Load:	$10^9\ \Omega$ test probe; 5.5 uA + ≤ 1 uA cable leakage

Current/Voltage/Connectors:

Current:	± (250 nA to 40 uA) ± 1%
Compliance Voltage:	± 5.5 kV
Ripple / Noise Voltage:	**Not specified at this time**
Overshoot / Undershoot:	Compliance voltage should not exceed ±6.0 kV
Settle Voltage / Time:	≈11 mS to switch (+19 mS for plasma to form)
Oscillator Frequency:	**FIXED** frequency ±10% (not variable with load)
Connector:	Connectronics 12 kV MIDGI Connector
High Voltage Return:	To case

Special Requirements:

A) Due to 30 pF load, an additional 30 uA output is required during a reversal event.
B) Output rate-of-change must be ≥ 1 kV/mS (w/30 pF load) at all times to satisfy our I_{OUT} requirements.
C) When reversing, the opposite current setting (via I_{CTRL}) may be a different magnitude.
D) Reversals occur every 0.6 seconds--no mechanical relays should be used in the reversing functions.

M. Lam DRAWN BY	04/24/98	**40 uA (±5.5 kV Compliant) Fast-Reversing Current Source Specification** TITLE	HEWLETT PACKARD
B. Crawford ENGINEER	04/24/98		
K. Horstman RELEASE TO PROD.	04/08/99		G1946-80058 PART NUMBER
SUPERSEDES DWG.	CURRENT REV A	PAGE 2 OF 4	**A-G1946-80058-2**

Regulation/Stability

Line Regulation:	≤ 0.1% of I_{OUT}
Load Regulation:	≤ 0.1% of I_{OUT}
Temperature Regulation:	≤ 250 PPM of I_{OUT}/°C
Short Term Stability[1]:	≤ 0.1% of I_{OUT} per hour
Long Term Stability:	≤ 0.5% of I_{OUT} per year

Control Lines:

Enable Line (TTL input) [ENABLE*]:[2]	High/open = Output OFF
Polarity (TTL input) [POL +/-*]:[3]	Low = Negative; High/open = Positive output
Polarity Input Impedance:	10 kΩ nominal
I1 Control (Input) [I CTRL]:	0 to 10 V_{DC}; Full Scale Output = 40 uA
I1 Control Input Impedance:	10 kΩ ± 0.1 kΩ

Monitor Lines:

Output Good (TTL output) [OUTPUT OK]:[4]	Low = Fault (control loop not in control, current not within bounds, etc.)
Positive Indicator Driver [POS IND*]	Open collector for LED, (Low = positive output)
Negative Indicator Driver [NEG IND*]	Open collector for LED, (Low = negative output)
Internal Reference (Output) [V REF]:	10 V_{DC} ± 0.025 V_{DC}
Reference Output Impedance:	≤ 10 kΩ; prefer < 2.2 kΩ
Voltage Output Monitor Line [V MON]:	0 to 10 V_{DC} = 5.5 kV Full Scale
Current Output Monitor Line [I MON]:	0 to 10 V_{DC} = 0 to 40 uA

Electrical Safety:

Case to HV RTN Isolation:	≤ 100 Ω || 0.10 uF (if using 0 Ω, please load a 0 Ω resistor)
LV RTN to Case Isolation:	≤ 100 Ω || 0.10 uF (if using 0 Ω, please load a 0 Ω resistor)
|Output| Decay Time to < 60V:	≤ 5 Seconds

Physical:

Refer to D-G1946-80058-1 "Physical Drawing" for details on the mechanical specification as well as the I/O ribbon cable pin out.

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1. Stability is specified using the standard bench test configuration specified in Appendix B. Temperature is a varied through the specified operating range. Stability is specified with constant temperature after a 1 hour warm-up.

2. Guaranteed enable is ≤ 0.5 V_{DC}; guaranteed disable is ≥ 1.5 V_{DC}.

3. Output is guaranteed Positive when Polarity Control is ≥ 2 V_{DC} and Negative for ≤ 0.65 V_{DC}.

4. **In fault**: output is guaranteed to be ≤ 1.1 VDC; **Not in fault**: output is guaranteed to be ≤ 4.3 V_{DC}.

Environmental:

Operating Temperature:	-5°C to 60°C
Storage Temperature:	-40°C to 70°C
Operating Altitude:	+15,000 to -1,000 feet
Storage Altitude:	+50,000 to -1,000 feet
Humidity (Operating):	5 to 95%, non-condensing
Humidity (Non-operating):	95%, 65°C non-condensing

Reliability:

Output is short circuit and arc protected.

Appendix A

Ripple and Noise Voltage is defined to include the following three catagories:

Table 1: Noise Definitions

Broadband Random Noise	Random, non-switch related noise on the high voltage output.
Broadband Switching Noise	Noise related to the oscillator, switching and feedback control circuitry other than ripple.
Ripple Noise	Noise associated with the rectified primary switching frequency.

Appendix B

The test hookup for qualification is as follows:

V_{IN}:	+24 V_{DC}
ENABLE*:	Low
I_{CTRL}:	0 to 10 V_{DC}
I_{OUT} Load:	As specified (both cases)
LV RTNs:	All tied to +24V RTN
HV RTNs:	Connected to suppressor
Case:	Externally wired to earth ground and +24 V RTN
Ambient Temperature:	23°C

M. Lam DRAWN BY	04/24/98	**40 uA (±5.5 kV Compliant) Fast-Reversing Current Source Specification**	HEWLETT PACKARD
B. Crawford ENGINEER	04/24/98		
K. Horstman RELEASE TO PROD.	04/08/99	TITLE	G1946-80058 PART NUMBER
SUPERSEDES DWG.	CURRENT REV A	PAGE 4 OF 4	**A-G1946-80058-2**

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REV	REVISIONS	APPROVED	DATE
A	Released from Rev 1 w/ changes per EC23-70263	K. Horstman	04/08/99

Description:

This specification sheet details the fast-reversing supply module used for the two zones of the ion source in LC/MS products. It is a voltage-controlled source whose outputs are ±6 kV_{DC} ($V_{CAPILLARY}$) and ±5.5 kV_{DC} ($V_{CHAMBER}$).

Input Control: Voltage controlled **Output Types:** Voltage sources, variable
Number of outputs: 2 outputs: (1) ± 6 kV, (2) ±5.5 kV tracking

Electrical Input:

Voltage:	$24 \pm 2\ V_{DC}$
Current:	$\leq 400\ mA_{DC}$
Ripple Current:	$\leq 30\ mA_{P-P}$

V1 Output:

Load Conditions:

System Load:	60 pF + (5 nA to 2 uA load current) Must meet all ripple requirements (below)
Bench Test Load:	$10^9\ \Omega$ test probe; 6 uA + ≤ 2 uA leakage Is **not** required to meet ripple requirements

Voltage/Current/Connector:

Voltage:	$\pm$ (0.2 to 6) $kV_{DC} \pm \approx 1\%$
Continuous Current @ steady-state full voltage:	2 uA (system) / 8 uA (bench)
Ripple / Noise Voltage:	$\leq 2V_{P-P}$ @ 2 uA[1]
Overshoot / Undershoot:	< 5% of output voltage change
Settle Voltage / Time:	Within 10 V of final voltage in ≤ 25 mS
Oscillator Frequency:	Any <u>one</u> frequency is acceptable (±10%), as long as it is consistent across all shipped units and for all load conditions
Connector:	Connectronics 15 kV SCID Connector
High Voltage Return:	Via case (or LV RTN)

Special Requirements

A) Due to 60 pF load, an additional 60 uA output is required during a reversal event.
B) Output reversing rate-of-change (via Polarity Ctl) must be ≥ 1 kV/mS (w/60 pF load).
C) When reversing, the opposite voltage setting (via V_{CTRL}) may be a different magnitude.
D) Output change within the same polarity (via V_{CTRL}) is DESIRED to be at least 0.8 kV/mS.
E) Reversals occur every 0.6 seconds--no mechanical relays should be used in the reversing functions.

---

1. Ripple voltage (Appendix A) is only specified at system load (2 uA) and **NOT** at bench load. This is to minimize output filter capacitance of the supply for fast reversal. Unit must be able to supply up to 8 uA at full voltage for bench testing.

Regulation/Stability

Line Regulation:	≤ 0.1% of V_{OUT}
Load Regulation:	≤ 0.1% of V_{OUT} (for "System Load" only)
Temperature Regulation:	≤ 300 PPM of V_{OUT}/°C
Short Term Stability[2]:	≤ 0.1% of V_{OUT} per hour
Long Term Stability:	≤ 0.5% of V_{OUT} per year

V2 Output:

Load Conditions

System Load:	60 pF + up to 40 uA continuous Must meet all ripple requirements (see below)
Bench Test Load:	10^9 Ω test probe; 5.5 uA + ≤ 2 uA leakage Should meet ripple requirements

Voltage/Current/Connector

Voltage:	±(0.2 to 5.5) kV_{DC} tracking 500 V closer to ground than V1 ("ΔV=500 V") **(Optional)** Use nAPCI pin to set V2=V1 ("ΔV=0 V")
Continuous Current @ steady-state full voltage:	40 uA
Ripple / Noise Voltage:	< 2 V_{P-P} @ 10 uA
Overshoot / Undershoot:	< 5% of output voltage change
Settle Voltage / Time:	Within 10 V of final voltage in ≤ 25 mS
Oscillator Frequency:	Any <u>one</u> frequency is acceptable (±10%), as long as it is consistent across all shipped units and for all load conditions
Connector:	Connectronics 12 kV MIDGI Connector
High Voltage Return:	Case

Special Requirements

A) Due to 60 pF load, an additional 60 uA output is required during a reversal event.
B) Output reversing rate-of-change (via Polarity Ctl) must be ≥ 1 kV/mS (w/60 pF load).
C) When reversing, the opposite voltage setting (via V_{CTRL}) may be a different magnitude.
D) Output change within the same polarity (via V_{CTRL}) is DESIRED to be at least 0.8 kV/mS.
E) Reversals occur every 0.6 seconds--no mechanical relays should be used in the reversing functions.

Regulation/Stability

Line Regulation:	≤ 0.1% of V_{OUT}
Load Regulation:	≤ 0.1% of V_{OUT} (for "System Load" only)
Temperature Regulation:	≤ 300 PPM of V_{OUT}/°C
Short Term Stability:	≤ 0.1% of V_{OUT} per hour
Long Term Stability:	≤ 0.5% of V_{OUT} per year

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2. Stability is specified using the standard bench test configuration specified in Appendix B. Temperature is a varied through the specified operating range. Stability is specified with constant temperature after a 1 hour warm-up.

Control Lines:

Enable Line (TTL input) [ENABLE*]:[3]	High/open = Both outputs OFF
Polarity (TTL input) [POL +/-*]:	Low = Negative; High/open = Positive output
Polarity Input Impedance:	10 kΩ nominal
V1 Control (Input) [V1 CTRL]:	0 to 10 V_{DC}; Full Scale = 6 kV
V1 Control Input Impedance:	≥ 100 kΩ
(Optional) nAPCI control (TTL input) [nAPCI*]:	High/open = "ΔV=500 V" (V2 closer to ground). When V1 < 500 V, V2 can be unregulated and stays between V1 and ground (to prevent arcing) Tolerance, steady state: ΔV = 500 V ± 10% Tolerance, during reversal: |ΔV| ≤ 800 V Low = "ΔV=0 V" (± 5%) (so V2 can be used as a "guard" voltage for V1 If implemented, add a jumper in the "unpotted" PCB area that can be removed after removing the cover (for engineering experiments, making this a "No Connect" between input signal and the circuitry)
V2 Control (Input):	Slaved to V1

Monitor Lines:

Output Good (TTL output) [OUTPUT OK]:[4]	Low = Fault (control loop not in control, voltage not within bounds, etc.)
Positive Indicator Driver [POS IND*]	Open collector for LED, (Low = positive output)
Negative Indicator Driver [NEG IND*]	Open collector for LED, (Low = negative output) (Both indicators should source 40 mA while active and are high/off when unit is disabled)
Internal Reference (Output) [V REF]:	10 V_{DC} ± 2% V_{DC} V REF is used to: (1) provide a reference for a low-cost resistor divider to drive V1 and V2 outputs and (2) test stability of the supply (e.g. V REF connected to V1 Control)
Reference Output Impedance:	≤ 10 kΩ; prefer < 2.2 kΩ
V1 Voltage Output Monitor [V1/V2 MON]:	0 to +10 V_{DC} ± 2%, Full Scale = 6 kV
V2 Voltage Output Monitor [V1/V2 MON]:	0 to +10 V_{DC} ± 2%, Full Scale = 6 kV NOTE: Bring V1 and V2 output monitors to an un-potted portion of the PCB so they can be switched into the V1/V2 MON output pin.
V1 Current Output Monitor [I1 MON]:	0 to +10 V_{DC} ± 2% = 0 to 2 uA
V2 Current Output Monitor [I2 MON]:	0 to +10 V_{DC} ± 2% = 0 to 40.96 uA

3. Guaranteed enable is ≤ 0.5 V_{DC}; guaranteed disable is ≥ 1.5 V_{DC}.

4. **In fault**: Output is guaranteed to be ≤ 1.1 V_{DC}; **Not in fault**: Output is guaranteed to be ≥ 4.3 V_{DC}.

Electrical Safety:

Case to HV RTN Isolation:	≤ 150 Ω || 0.10 uF (if using 0 Ω, please load a 0 Ω resistor)
LV RTN to Case Isolation:	≤ 150 Ω || 0.10 uF (if using 0 Ω, please load a 0 Ω resistor)
|V1| Decay Time to < 60V:	≤ 5 Seconds
|V2| Decay Time to < 60V:	≤ 5 Seconds

Physical:

Refer to D-G1946-80059-1 "Physical Drawing" for details on the mechanical specification as well as the I/O ribbon cable pin out.

Environmental:

Operating Temperature:	-5°C to 60°C
Storage Temperature:	-40°C to 70°C
Operating Altitude:	+15,000 to -1,000 feet
Storage Altitude:	+50,000 to -1,000 feet
Humidity (Operating):	5 to 95%, non-condensing
Humidity (Non-operating):	95%, 65°C non-condensing

Reliability:

Outputs are short circuit and arc protected.

Appendix A

Ripple and Noise Voltage is defined to include the following three catagories:

Table 1: Noise Definitions

Broadband Random Noise	Random, non-switch related noise on the high voltage output.
Broadband Switching Noise	Noise related to the oscillator, switching and feedback control circuitry other than ripple.
Ripple Noise	Noise associated with the rectified primary switching frequency.

Appendix B

The test hookup for qualification is as follows:

V_{IN}:	+24 V_{DC}
Enable Line:	Low
V1 Control Input:	0 to 10 V_{DC}
V1 Output Load:	(As specified)
LV commons:	All tied to +24 V rtn
HV common:	
Case:	Floating
Ambient Temperature:	23°C

M. Lam DRAWN BY	04/24/98	**±6 kV Fast-Reversing Dual Output Voltage Source Specification** TITLE	HEWLETT PACKARD
B. Crawford ENGINEER	04/24/98		
K. Horstman RELEASE TO PROD.	04/08/99		G1946-80059 PART NUMBER
SUPERSEDES DWG.	CURRENT REV A	PAGE 5 OF 5	**A-G1946-80059-2**

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REV	REVISIONS	APPROVED	DATE
A	Released from Rev 1 w/ changes per EC23-70263	K. Horstman	04/08/99

M. Lam DRAWN BY	04/24/98	**±10 kV Fast-Reversing Voltage Source Specification** TITLE	HEWLETT PACKARD
B. Crawford ENGINEER	04/24/98		
K. Horstman RELEASE TO PROD.	04/08/99		G1946-80060 PART NUMBER
SUPERSEDES DWG.	CURRENT REV A	PAGE 1 OF 4	**A-G1946-80060-2**

Description:

This specification sheet details the fast-reversing supply module used for the High Energy Dynode (HED) in LC/MS products. It is a voltage-controlled high-voltage power source (±10 kV_{DC}).

Input Control: Voltage controlled **Output Type:** Voltage source, variable
Number of outputs: 1 output: (1) ± 10kV

Electrical Input:

Voltage:	24 ± 2 V_{DC}
Current:	≤ 300 mA_{DC}
Ripple Current:	≤ 30 mA_{P-P}

V1 Output:

Load Conditions:

System Load:	19 pF (assume ≤ 2 uA leakage at full voltage) Must meet all ripple requirements (below)
Bench Test Load:	10^9 Ω test probe; 10 uA + ≤ 1 uA cable leakage Does **not** have to meet ripple requirements

Voltage/Current/Connectors:

Voltage:	± (0.5 to 10) kV_{DC} ± 1%
Continuous Current @ steady-state full voltage:	2 uA (system) / 11 uA (bench)
Ripple / Noise Voltage:	< 1 V_{P-P} @ 2 uA[1]
Overshoot / Undershoot:	< 5% of output voltage change
Settle Voltage / Time:	Within 10 V of final voltage in ≤ 25 mS
Oscillator Frequency:	**FIXED** frequency ±10% (not variable with load)
Connector:	Connectronics 15 kV SCID Connector
High Voltage Return:	Molex plug on flying lead[2]

Special Requirements:

A) Due to 19 pF load, an additional 19 uA output is required during a reversal event.
B) Output reversing rate-of-change (via Polarity Ctl) must be ≥ 1 kV/mS (w/19 pF load).
C) Output change within the same polarity (via V_{CTRL}) needs to be at least 0.001 kV/mS (1 V/mS)
D) Reversals occur every 0.6 seconds--no mechanical relays should be used in the reversing functions.

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1. Ripple voltage (Appendix A) is only specified at system load (2 uA@ max. output voltage) and **NOT** at bench load. This is to minimize output filter capacitance of the supply. Unit must be able to supply up to 11 uA at full voltage for bench testing.

2. The high voltage return is a green wire on pin 2 of the Molex Minifit Jr. plug. Its intended use is to return energy generated from an arc back to the supply.

Regulation/Stability

Line Regulation:	≤ 0.1% of V_{OUT}
Load Regulation:	≤ 0.1% of V_{OUT} (for system load only, 0-2 uA)
Temperature Regulation:	≤ 300 PPM of V_{OUT}/°C
Short Term Stability[3]:	≤ 0.1% of V_{OUT} per hour
Long Term Stability:	≤ 0.5% of V_{OUT} per year

Control Lines:

Enable Line (TTL input) [ENABLE*]:[4]	High/open = Output OFF
Polarity (TTL input) [POL +/-*]:[5]	Low = Negative; High/open = Positive output
Polarity Input Impedance:	10 kΩ nominal
V1 Control (Input) [V CTRL]:	0 to 10 V_{DC}; Full Scale Output = 10 V_{DC}
V1 Control Input Impedance:	10 kΩ nominal

Monitor Lines:

Output Good (TTL output) [OUTPUT OK]:[6]	High = Output OK, Low = Fault (control loop not in control, voltage not within bounds, etc.)
Internal Reference (Output) [V REF]:	10 V_{DC} ± 0.025 V_{DC}
Reference Output Impedance:	≤ 10 kΩ; prefer < 2.2 kΩ
V1 Voltage Output Monitor Line [V MON]:	0 to 10 V_{DC} = Full Scale
V1 Current Output Monitor Line [I MON]:	0 to 10 V_{DC} = 0 to 2 uA (Can be > 10 V_{DC} for ≥ 2 uA; clamping not required)

Electrical Safety:

LV RTN to HV RTN Isolation:	100 Ω || 0.47 uF nominal
LV RTN to Case Isolation:	100 Ω || 0.47 uF nominal
|V1| Decay Time to < 60V:	≤ 5 Seconds

Physical:

Refer to D-G1946-80060-1 "Physical Drawing" for details on the mechanical specification as well as the I/O ribbon cable pin out.

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3. Stability is specified using the standard bench test configuration specified in Appendix B. Temperature is a varied through the specified operating range. Stability is specified with constant temperature after a 1 hour warm-up.

4. Guaranteed enable is ≤ 0.5 V_{DC}; guaranteed disable is ≥ 1.5 V_{DC}.

5. Output is guaranteed Positive when Polarity Control is ≥ 2 V_{DC} and Negative for ≤ 0.65 V_{DC}.

6. **In fault**: output is guaranteed to be ≤ 1.1 VDC; **Not in fault**: ≥ 4.3 V_{DC}.

Environmental:

Operating Temperature:	-5°C to 60°C
Storage Temperature:	-40°C to 70°C
Operating Altitude:	+15,000 to -1,000 feet
Storage Altitude:	+50,000 to -1,000 feet
Humidity (Operating):	5 to 95%, non-condensing
Humidity (Non-operating):	95%, 65°C non-condensing

Reliability:

Output is short circuit and arc protected.

Appendix A

Ripple and Noise Voltage is defined to include the following three catagories:

Table 1: Noise Definitions

Broadband Random Noise	Random, non-switch related noise on the high voltage output.
Broadband Switching Noise	Noise related to the oscillator, switching and feedback control circuitry other than ripple.
Ripple Noise	Noise associated with the rectified primary switching frequency.

Appendix B

The test hookup for qualification is as follows:

V_{IN}:	+24 V_{DC}
ENABLE*:	Low
V CTRL:	0 to 10 V_{DC}
V OUT Load:	As specified (both cases)
LV RTNs:	All tied to +24V rtn
HV RTNs:	Connected to suppressor
Case:	Externally wired to earth ground and +24 V RTN
Ambient Temperature:	23°C

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REV	REVISIONS	APPROVED	DATE
A	AS RELEASED PER PC23-5710	J. FOOTE	5/21/96

CARL PICCIOTTO DRAWN BY	05/21/96	**G1099-60001 Log Amplifier Theory of Operation**	HEWLETT PACKARD
C. PICCIOTTO ENGINEER	05/21/96		
J. FOOTE RELEASE TO PROD.	5/21/96	TITLE	G1099-60001 PART NUMBER
SUPERSEDES DWG.	A CURRENT REV	Page 1 of 16	**A-G1099-60001-5**

G1099-60001 Logarithmic Signal Amplifier

General Specifications

Max. input current	50µA (current flowing OUT of amplifier; i.e., electrons flowing IN)
Low-end quantization step size	~3pA
High-end resolution	0.262% of signal level
Effective Bandwidth	4kHz (2-pole input filter, with poles at 4.3kHz and 66kHz)
Max. linearity error (measured by the 15µA/15nA count ratio)	+/- 1.5% over normal operating temperatures (Measured +/-1%, in the 10° - 30° range)
Typical std. dev. of open-input noise	~3-4 (with cable connected at the log-amp, and disconnected (and shielded) at the other end)
Typical open-input count	30-60
Input resistance	737.2kΩ +/– 1%
Max. input offset voltage (ignoring drop across input filter)	0.4mV over normal operating temperatures (Specification of AD820BR op-amp)
Min. ADC conversion time	10µs (taken from ADC specifications)
Max. ADC data access time (including on-board delays other than the ADC itself)	163.2ns
Max. EEPROM read access time	200ns (valid data following chip enable)
Min. chip-enable/write pulse-width for writing to the EEPROM	100ns
Min. device-select pulse-width for writing to the calibration DACs	~230ns (180ns + ~50ns max. U7 Schmitt-trigger delay)

An additional feature on the board is a triangle-wave generator. Upon actuation, the circuit sums a triangular wave of current into the input. The purpose is to provide a first-shot at diagnosing system problems, as well as to test-out the log-amp itself, without the inconvenience of hooking-up external power supplies or signal generators.

Log Math

The number read off the log-amp's 12-bit ADC is proportional to the logarithm of the input current. This means that before the abundance values can be properly processed, they must be 'unlogged', or exponentiated, to a linearized value.

The formula for unlogging is:

$$COUNT = 370\left(2^{\frac{ADC}{265}} - 1\right), \quad (1)$$

where COUNT is the unlogged value, and ADC is the 12-bit integer ranging from 0 to 4095.

The coefficients 370 and 265 were chosen to approximate a one-to-one relationship between the ADC values and the unlogged abundance counts at the low-end (so that we're not 'throwing-away' ADC bits), and to at-least preserve the high-end resolution obtained in the 5972. As it turns out, the high-end resolution is now *slightly* better than that seen on the 5972, even though the full-scale range is over twice as high.

Currently, SmartCard performs the unlog function with a look-up table, generated when SmartCard is initialized.

How Log-Amps Work

Log-amps generate voltages proportional to the logarithm of their inputs (typically currents).

The function is achieved by taking advantage of the exponential relationship between current and voltage in a bipolar transistor. Specifically, the collector current I_c may be expressed as an exponential function of the emitter-base voltage V_{eb} (for a PNP transitor) as follows:

$$I_C = I_S e^{\frac{V_{eb}}{nV_T}}, \quad (2)$$

where I_s is the saturation current, V_T is the thermal voltage, typically~25mV, and n is a contant near unity. In reality there are other terms to the equation, but they're quite small, especially if care is taken to ensure that the collector-base voltage is held near zero, as is the case with this implementation.

Rearranging and solving for V_{eb},

$$V_{eb} = nV_T \ln\left(\frac{I_C}{I_S}\right) \quad (3)$$

Why a Log-Amp?

The dynamic range of the signal channel, ignoring issues of minimum signal-to-noise ratios and looking strictly at the pure range of quantization, is 50µA/3pA, or about 16.7Million. This number would require 23 bits to quantize uniformly. At a sampling rate of16µs, it should be immediately obvious that a simple-minded approach of using a 23-bit ADC would be impractical and very expensive, if even possible.

Logarithmic amplifiers provide a relatively inexpensive way to acquire signals of high dynamic range at a reasonably fast rate, when the required resolution may be expressed in a relative sense; that is, the minimum required resolution may be given as a percentage of the signal level, and not as a fixed absolute, so that the absolute resolution may be allowed to decreased with larger signals. This is the case with mass spectrometry.

By amplifying the LOGARITHM of the input current, andquantizing with a mere 12 bits, we can achieve this dynamic range, at the required sampling rate.

The disadvantage of ANY band-limited sampling amplifier, such as this logarithmic amplifier, is the problem of "memory" from sample to sample, causing smearing and loss of resolution. Increasing the bandwidth and increasing the sampling rate reduces the problem, but does not eliminate it. Still, it remains to be seen whether the weakest link in resolution is the signal amplifier, or thequadrupole mass filter itself.

There are other amplifier topologies, such as gain-ranging integrators, pulse-counters, etc., all with their own advantages and drawbacks.

Herein lies plenty of food for thought, which should be eaten somewhere else.

Overview

The log-amp is a piggy-back board used by both 7UP and Sprite for amplifying andquantizing the mass spectrometers' ion currents. The board plugs onto motherboards in each instrument, communicating through SmartCard's MSE bus, passing abundance counts over 12 of the 16 bits available onMSE's data bus.

Allowable signals range from the lowpA to 50µA. At the low-end the quantization step size is ~3pA, and at the high-end it's~130nA, or 0.262% (expressed as a percentage of signal level). For comparison, the 5972 log-amp has a low-end quantization step size of ~3pA, a high-end resolution of 0.270%, and a full-scale range of20µA.

A dual 8-bit multiplyingDAC is used to adjust the amplifier's gain and offset, affecting calibration for both linearity (gain adjust) and full-scale range (offset adjust). Calibration of the amplifier is done on the manufacturing line under computer control using an external precision current source. Ratios of currents are injected into the input, and the log-amp's gainDAC is adjusted until the resultingunlogged (see *Log Math* below) count ratios come into line, and the offset DAC is adjusted to bring the absolute levels in line. The calibration data (two bytes: gain, offset) are stored in the on-board EEPROM. On system initialization, SmartCard reads the calibration values from theEEPROM, and writes them back to the multiplyingDACs.

So now we see a logarithmic relationship between voltage and current, a relationship utilized by the log-amp. In a nutshell, the log-amp varies the emitter-base voltage of the logging transistor Q2a until its collector current matches the input current, and then it measures and amplifies the compliant emitter-base voltage.

How it works: U3's goal in life, like any well-behaved negatively fed-back op-amp, is to ensure a virtual short across its inputs. As electrons (signal currents) flow toward the inverting input, the potential at that point is driven down, causing the op-amp output to rise in voltage. This rise in voltage causes a higher emitter voltage at Q2a, hence increasing Q2a's emitter-base drop, turning Q2a on a little bit harder. Current increases, then, through Q2a, which pulls electron (negative) current away from the op-amp input, until a virtual short once-again exists across the op-amp inputs.

The end-result is that input currents (negative) flow past the op-amp and directly into the collector of the logging transistor, while the op-amp establishes the corresponding compliant emitter-base voltage. The voltage is passed through an additional transistor (for temperature compensation... more on that later), buffered, offset and amplified, and then sent to the ADC.

Signal Flow

Signal currents flow through the front-end filter R_3,R_6,C_2,C_3 (actually the currents flow OUT, since electrons are flowing IN), and through the logging transistor Q2a. The op-amp U3 establishes the compliant log voltage at the emitter of Q2a. This voltage is subtracted by the drop across the emitter-base junction of Q2b (established by the constant current of ~500nA) and then buffered by U5b. The purpose of Q2b is to provide compensation for temperature affects (see *Temperature Compensation*, below).

U5a magnifies this tiny voltage by a factor of about 25 (or as much as 32, depending on the setting of DAC U1 (see next paragraph)) to bring it into the 10V range of the ADC U6. R_1, R_4, R_{14}, R_{15}, R_{16}, and R_{21} are chosen very carefully to establish the necessary nominal gain and offset and calibration ranges of the U5a stage. U6 then quantizes the voltage and asserts the 12-bit logged abundance words onto the data bus (when requested by the off-board timing signals).

The dual 8-bit multiplying DAC U1, with help from U2 (for converting U1's output currents to voltages), adjusts the offset and gain of the amplifier U5a by summing fixed voltages (for the offset calibration), and voltages proportional to the signal (for the gain calibration), to the inverting input of U5a. The DAC settings of U1 are fixed, set only during SmartCard initialization.

+10V_THERM is a voltage proportional to Kelvin temperature, nominally +10V. More on this in *Temperature Compensation*.

You may be wondering about the curious configuration involving R_1 and R_4, stuck in the circuit of U2b. I needed a way to add an offset of about ~+5.2V to the output of U5a, proportional to +10V_THERM. To do this, we needed to sum a *negative* current to the inverting input of U5a, which means we needed a *negative* voltage, and I didn't want to add the expense of an additonal op-amp simply to invert this signal.

So instead, U2b was 'borrowed' to provide the inversion. Analyzing the circuit, if we define V_1 as the voltage at the FDBK$_B$ output of U1, and V_2 as +10V_THERM, and R_{DAC} as the internal resistance of the DAC (somewhere between 8KΩ and 15KΩ), then we get the following expression for the voltage at the output of U2b:

$$V_o = V_1\left(1 + \frac{R_1}{R_{DAC}} + \frac{R_1}{R_4}\right) - V_2\frac{R_1}{R_4} \qquad (4)$$

The last term, $-V_2R_1/R_4$, accomplishes what we need. Without R1 and R4 in the circuit, the output V_O would simply equal V_1; in other words, V_1 is the 'normal,' unmodified output of the DAC. Ideally, with R_1 and R_4 in place, we'd really like to see $V_O = V_1 - V_2R_1/R_4$. If we keep R_1 small w.r.t. R_{DAC} and R_4, then we don't stray too far from this ideal. Note that we can easily calibrate the amplifier to make-up for the error; it's the temperature drifts of $(1 + R_1/R_{DAC} + R_1/R_4)$ that are important here, and that we've minimized by keeping R_1 as small as practical.

Bandwidth

The biggest limiter to the log-amp's bandwidth is the intrinsic capacitance of Q2a, the logging transistor.

At low signal levels, the "resistance" of the transistor is very large. That is, a change in emitter-base voltage over a change in collector current is very large. A little calculus shows:

$$\begin{aligned}\frac{\partial V_{eb}}{\partial I_C} &= \frac{\partial}{\partial I_C}\left[nV_T \ln\left(\frac{I_C}{I_S}\right)\right] \\ &= nV_T\frac{I_S}{I_C}\frac{1}{I_S} \\ &= \frac{nV_T}{I_C},\end{aligned} \qquad (5)$$

where V_T is the thermal voltage, typically ~25mV. This figure naturally gets large when I_c heads down into the picoamps.

Any capacitance across this transistor (internal or external) will form a time constant with this "resistance", limiting the log-amp's bandwidth, in the region of operation where the dV_{eb}/dI_c is high; namely, at the lowest currents.

The lowest current the log-amp will see is set by a constant bias current. The voltage divider formed by R_9, R_{10}, and R_{12} establishes a voltage that's about -24.9mV (ignore Q4 at the moment... assume it's completely off). Resistors R_7 and R_8, connected in series to form 20MΩ, see this voltage, and thus force a constant ~1.24nA to sum into Q2a's collector. Thus, the lowest currents Q2a should ever experience will be when there is no input current, and only the 1.24nA bias current remains.

ASIDE: The input-offset voltage of U3 is a potential source of error in establishing the bias current, since the voltage seen by R_7 and R_8 is offset by it; however, the input-offset voltage is maximally +/-0.4mV (in ordinary operating temperatures), giving a maximum error of +/-0.4mV / 20MΩ, or +/-20pA, so the error is minimal.

By increasing the bias current through the logging transistor from the 5972 level of ~450pA to ~1.24nA, we were able to push up the bandwidth. There is evidence of possibly being able to reach up to 6.5kHz at this bias current. However, since we currently aren't capable of sampling faster than 16µs, the bandwidth of the input filter must be restricted to 4kHz, to ensure maximum integration of the signal currents, and thus preserve our signal-to-noise ratio (with a higher bandwidth, we'd lose too much of the signal through premature decay). A simple way of looking at this is that our bandwidth must match our sampling rate. It's an issue somewhat related to the Nyquist criterion, but it's really not the same thing.

IMPORTANT NOTE: to avoid distortion of the signals, the front-end filter MUST dominate the bandwidth, the reason being that signals downstream of the filter are in the logarithmic domain, so any linear filtering would result in non-linear distortion.

The two-pole front-end filter (R_3,R_6,C_2,C_3) was designed to exhibit a step-response equal to a single-pole 4kHz filter. The two poles are at ~4.3kHz and ~66kHz, which yield such a response.

The poles may be derived through painful nodal analysis. Luckily for you I've slogged through the pain! The poles (in radians/sec) may be obtained from:

$$\omega_1, \omega_2 = \frac{R_6C_3+R_6C_2+R_3C_2 \pm \sqrt{(R_6C_3+R_6C_2+R_3C_2)^2-4R_6C_3R_3C_2)}}{2R_6C_3R_3C_2} \quad (6)$$

and the step-response, after a time t, derived using LaPlace transforms, is given by:

$$StepResp = \frac{\omega_1\omega_2}{\omega_1-\omega_2}\left(\frac{1-e^{-\omega_2 t}}{\omega_2} - \frac{1-e^{-\omega_1 t}}{\omega_1}\right) \quad (7)$$

Note that ~50pF cable capacitance must be added to C_2.

The filter exhibits a step-response of 0.63 (i.e., it settles to 63%) in 40µs, just like a single-pole 4kHz filter.

For <u>better electronic noise performance</u>, a 1pF capacitor (C_4) was placed across the logging transistor, to cut down the transistor's ability to amplify higher frequencies. A side-effect of doing this is that, at the lowest signal levels, the bandwidth is not dominated by the input filter, but by the logging transistor, such that the half-power point is reached at about 4kHz, not 4.3kHz. This means that there is a subtle bandwidth reduction at the <u>absolute lowest</u> levels. Yes, this means we've violated the commandment that the input filter must ALWAYS dominate the bandwidth; however, distortion should not really be a concern, since the log and linear curves look very similar at these levels. Also, a slight bandwidth reduction at these low levels may not be such a bad thing, since the ion currents are noisiest at the lowest levels and should benefit from more integration.

If anyone is TOO offended, the capacitor can be removed, at the expense of increased electronic noise (a ~50% increase in standard deviation of open-input noise). The amplifier should still be stable, but it's definitely worth verifying.

C_9, in the feed-back circuit of U5a, limits the bandwidth of the final gain stage to about 35kHz. The log-amp signal is band-limited by the 2-pole front-end filter, so a 35kHz cut-off should not intefere with (distort) the

signal any appreciable amount. Its purpose is to filter any higher-frequency noise originating from within the log-amp electronics.

Stability and Noise

Log-amps are notoriously difficult to stabilize. The reason is that the loop response keeps on changing everytime the signal level moves! Having a transistor in the feedback path of an op-amp is just asking for trouble!

The logging transistor Q2a can be modeled as a varying resistance in parallel with a capacitance. The effective resistance, as developed above under ***Bandwidth***, is approximated by nV_T/I_c, clearly affected by changes in collector current. The capacitance in this model is fixed (don't bother looking at the transistor specification sheets for a collector-emitter capacitance, because you won't find it), somewhere <10pF.

In an effort to stabilize the circuit, U3 was chosen for its high phase margin (as well as low input-offset voltage, low input bias currents, low equivalent input noise voltage, ability to recover quickly from railing, and its low price). The loop gain was minimized with the resistor-divider R_{39} and R_{36}. The log-amp tended to oscillate at higher currents (and at pretty high frequencies), so C_{21} was added to add a high frequency zero to the loop gain. Adding a little eye-of-newt helped.

Still, the log-amp has a sensitive spot in the ~30nA to ~150nA region. To minimize the likelihood of oscillation, the impedance looking back towards the input filter had to be adjusted in creative ways...see the Engineering Report for details.

It is important to note here that, by changing the filter components, we change not only the stability of the circuit, but we influence the level of electronic noise. The higher the capacitance in the filter, the higher the noise levels. Why? I'll tell you: the op-amp has an inherent level of voltage noise present at its inputs, which is amplified most effectively by low impedances at high frequencies: high capacitance! So it is wise to keep the capacitance down. Fortunately we were able to keep the capacitance quite low, resulting in noise levels superior to those of previous log-amps.

Unfortunately, to achieve low capacitance, the total resistance of the filter had to be raised. This means that the voltage looking into the log-amp input, at high currents, can be quite high (potentially greater than -30V), effectively reducing the ability of the electron-multiplier's collection-cup to attract electrons. So, high signal levels *may* become attenuated, leading to linearity issues. We haven't really seen experimental evidence of this yet.

STABILITY TESTING NOTE: On the manufacturing floor, stability is verified by injecting currents in the regions of difficulty noted above, and verifying that the unlogged abundances look right. Also, a good way of visually verifying stability is to run the triangular-wave self-test, which will not run properly if the log-amp is unstable.

Temperature Compensation

As you may recall from the section *How Log-Amps Work*, the log voltage is given by

$$V_{eb} = nV_T \ln\left(\frac{I_C}{I_S}\right). \quad (3)$$

There are two temperature gotchas to watch out for. The saturation current I_s is sensitive to temperature, and the thermal voltage V_T, as the name implies, is also sensitive to temperature. V_T is actually kT/q, where k is Boltzmann'sConstant, q is the electron charge in Coulombs, and T is the temperature in degrees Kelvin.

Q2a, the logging transistor, is half of a transistor pair. Two PNP transistors share the same package, so they are in very good thermal contact. The other half of Q2, Q2b, is diode-connected, and has a constant current of ~500nA flowing through it, regulated by R20 and the -5V supply. The 500nA current will fluctuate slightly with signal level and temperature, but the approximation appears to be more than adequate.

The two transistors are connected in series, so that the buffer U5b sees the difference in emitter-base voltages of the two transistors Q2. This voltage is then amplified by U5a and sent to the ADC.

With the log voltage equation (3) re-written as

$$V_{eb} = nV_T(\ln(I_c) - \ln(I_s)), \quad (8)$$

the difference in emitter-base voltages may be written:

$$V_{DIFF} = nV_T(\ln(I_{c1}) - \ln(I_{c2})). \quad (9)$$

We are assuming that I_s and nV_T are matched for both transistors Q2, and we've designated the two collector currents as I_{c1} and I_{c2}. Notice that the pesky temperature-sensitive saturation currents are cancelled out.

What remains is to compensate for V_T, which varies directly with Kelvin temperature. Classically, this is done with a thermistor acting as a denominator term in an op-amp stage. We take a different approach, one that at the time of this writing is undergoing a patent search. By varying the reference voltage to the ADC proportionally to Kelvin temperature, we are able to track the temperature-induced movements of (9), and hence cancel-out the temperature variation.

Why does this work? ADC's use their reference voltage as a guage to determine the magnitude of the input signals. For a 12-bit ADC, for example, the ADC will convert a voltage V_{sig} into a 12-bit number with the expression V_{sig}/V_{ref} * 4096, rounded to an integer. This means that the converted number is inversely proportional to V_{ref}; hence, if V_{ref} is made to vary in direct proportion to Kelvin temperature, then the temperature variations of V_{sig}, in this case an expression proportional to (9), will be matched by V_{ref}, and thus be cancelled.

In this case, the hypothetical V_{ref} of the above paragraph is the signal +10V_THERM, generated by the circuit of U8b and the transistor pair Q1. +10V_THERM is consequently the voltage reference for the ADC U6. A side-affect of this is that any component of the input signal to U6 *must be referenced off +10V_THERM,* or the

scaling will drift around with temperature. In other words, in an ironic twist, all signal voltages *must* drift with temperature to track the reference voltage! Notice that +10V_THERM is therefore the reference to the calibration offset circuits (by U1 and U2).

+10V_THERM, as the name implies, is nominally 10V, and is designed to vary directly with Kelvin temperature, approximately 34mV/degC near room remperature. It operates by forcing constant currents through each transistor of the Q1 PNP pair, subtracting the resulting emitter-base voltages, and amplifying the difference, ending-up with a voltage given by an expression like (9), but amplified by a factor of about 130. So, as before, the saturation currents of Q1a and Q1b cancel each other out, and the only temperature-dependent term we're left with is proportional to V_T, which is exactly what we want.

Q1b sees about 1mA of current, while Q1a sees 50µA. Q1b is diode-connected, and is fed ~1mA through its emitter by R_{28} and +10V_REF (generated by U6). The current will change slightly as Q1b's emitter voltage drifts, but only by a small amount, since any drifts will be small compared to 10V. Also, the current being stolen away from Q1b to the emitter of Q1a is held essentially constant (and comparatively tiny) so it shouldn't be a source of error. Since we need Q1b's COLLECTOR current to be a constant, Q1b's beta parameter comes into the picture, so that drifts in beta may be a slight source of error; however, at 1mA the beta is pretty high (>100, I'd guess), so temperature-induced variations in base currents should be very small in proportion to 1mA.

Q1a has a well-regulated 50µA of current flowing through its collector. The current is regulated by U8b, whose output pulls down (through R41) on the resistor-divider R26 & R27, turning on Q1a, until the voltage at Q1a's collector reaches zero. Thus, determined by R_{11} and the -5V reference, and unperturbed by the insignificantly small current flowing into U8b's non-inverting input, the collector current of Q1a is regulated to 50µA.

Since the two transistors of Q1 are connected in series, the difference in their emitter-base voltages appears at the base of Q1a. The action of the resistor-divider R_{26} & R_{27} magnifies the tiny base voltage by a factor of about 130, to get to the ~ +10V level, at the point at which +10V_THERM is taken. More than 1mA flows through the divider so any µA-level current flowing out of the base of Q1a should give no significant errors.

We have realized a fairly complex function with a single op-amp.

With the exception of C_{28}, which is needed for closed-loop stability, the extra capacitors thrown around are manifestations of paranoid attempts to keep noise levels done. The noise levels haven't necessarily been shown to be a problem, and it hasn't been shown that the extra filtering makes any difference,... so it goes.

Since +10V_THERM is meant to counter thermal variations of Q2, Q1 and Q2 are placed in close thermal contact on the PC-board.

Notes on Calibration

Repeated from *Overview*:

A dual 8-bit multiplyingDAC is used to adjust the amplifier's gain and offset, affecting calibration for both linearity (gain adjust) and full-scale range (offset adjust). Calibration of the amplifier is done on the manufacturing line under computer control using an external precision current source. Ratios of currents are injected into the input, and the log-amp's gainDAC is adjusted until the resulting unlogged count ratios come into line, and the offset DAC is adjusted to bring the absolute levels in line. The calibration data (two bytes: gain, offset) are stored in theon-board EEPROM. On system initialization,SmartCard reads the calibration values from theEEPROM, and writes them back to the multiplyingDACs.

It may be useful to discuss why we need to calibrate, and what the two calibration adjustments are really doing to the amplifier's transfer function. In simple terms, the log voltage can be an expressed as a logarithm of the input current, scaled by a gain (G) factor and offset by an offset (O) adjustment:

$$V_{LOG} = G(\ln(I_{in}) + K) + O, \qquad (10)$$

where K is a constant. G and O, of course, are representatives of the parameters adjusted during calibration.

Recall the anti-log equation

$$COUNT = 370\left(2^{\frac{ADC}{265}} - 1\right), \qquad (1)$$

used by SmartCard to linearize the abundance counts. Using the ADC quantization equation ADC = $V_{LOG}/10 * 4096$ (ignoring the discretization), and applying (1) to (10), we get

$$\begin{aligned} COUNT &= 370\left(2^{\frac{V_{LOG}}{10}\frac{4096}{265}} - 1\right) \\ &= 370(2^{1.55V_{LOG}} - 1) \\ &= 370\left(2^{1.55\left(G\left(\ln\left(I_{in}\right)+K\right)+O\right)} - 1\right) \\ &= 370\left(2^{1.55(GK+O)} I_{in}^{1.55G(\ln(2))} - 1\right) \\ &= 370\left(2^{1.55(GK+O)} I_{in}^{1.071G} - 1\right) \end{aligned} \qquad (11)$$

Of course, the granularity of the quantization is left-out, but the general idea is represented.

For the abundance counts to be linear with input current, the exponent 1.071G MUST equate to unity. When we are adjusting the gain calibration, we are effectively adjusting G until we achieve this result. We know we've reached the target when ratios of applied input currents yield equivalent ratios of abundance counts, remembering to subtract-off the constant bias count of about 50.

(11) shows that the offset adjustment O acts to scale the abundance counts. So, once we'velinearizedthe response by adjusting G, we need to adjust the count scaling by setting O. A constant current is injected (typically15µA) and the offset adjusted until the correct abundance count is reached. For example, if the input current is set to 15µA, the abundance count target is 15µA/(3pA per count), or 5Millioncounts.

In summary: calibration is achieved by first adjusting the gain until the amplifier is linear, and then adjusting the offset until the abundance scaling is correct.

Ordinarily, the gain calibration adjustment should have enough range to calibrate any log-amp. However, if the gain adjustment is pegged at one extreme and the amplifier still isn't calibrated, and it appears that calibration could be achieved with further adjustment (i.e., it doesn't appear to be a lost cause), then resistor R_{60} or R_{61} may be removed to adjust the level of +10V_THERM, which should bring the gain adjustment in-line. If the gain adjustment is pegged at 255, then removing R_{60} would lower +10V_THERM, requiring less gain. If the gain adjustment is pegged at 0, then removing R_{61} would raise +10V_THERM, requiring more gain.

Triangle-Wave Test Circuit

The triangle-wave circuit *sums* a triangle-wave of current into the input of the log-amp. The idea is to provide an easy way of 'faking' real signals, to provide a first-shot at diagnosing system problems, as well as to test-out the log-amp itself, without the inconvenience of hooking-up external power supplies or signal generators. It should be stressed that the triangular wave is *summed* to whatever actual signal currents happen to be present.

U9, U8a, Q4, Q5, Q6, Q7, and a whole bunch of associated components make up the triangle-wave generator circuit, including a 'current-source switch' for summing the waveform into the log-amp's input.

When 'SIG_CHAN_TEST' is pulled high, Q7 turns off, so Q6 turns off, and the triangle-wave circuit is allowed to run. U9a is configured as an integrator, storing charge in C23 and hence ramping-up its output. U9b is used simply as a comparator. When the ramping voltage at the non-inverting input trips the threshold set at the inverting input, the op-amp output will swing from one rail to the other (kind of violent, yes), turning-on or switching-off Q5. R43, R46, and CR1 limits the gate-source voltage of Q5 to a reasonable level during the 'turn-on' phase, when the output of U9b is railed positive (Q5 is a JFET, a depletion-type device, and conducts the most current at a V_{GS} of zero, not +15V, so we need to limit the positive-going swing). Q5 switches the threshold voltage at the inverting input of U9b, and also switches the slope of the ramping voltage. When the threshold is at a high voltage, the ramp slope is positive, and when the threshold is at a low voltage, the ramp slope is negative, so that the ramping voltage is always approaching the threshold. Q5 is able to affect the ramp's slope by changing the polarity of the voltage to the right (on the schematic) of R_{32}, thereby changing the polarity of the current flowing through R_{32} and to the integrator.

Solving for this network of resistances was no easy task. The trick was to set the thresholds in the right place, while at the same time ensuring that the two ramp slopes were of equal magnitude and opposite polarity, so that the triangle wave would be symmetric.

C31 was added to slow-down the turn-on, turn-off points of Q5, because it was determined that the switching was too violent, causing glitching in the -5V reference, ultimately causing glitches in the signal channel, so that the triangle-wave would have glitches at its top and bottom corners. The result is a triangle wave with smoothly rounded corners, and less accurately defined tops and bottoms. The waveform was never intended for highly precise measurements anyway.

The triangular-wave of voltage present at the non-inverting input of U9b now has to be converted to a current and injected into the input of the log-amp. U8a inverts and reduces the triangle wave by a factor of R_{25}/R_{29} to form a triangle wave at the junction of R_{25} and R_{31}. It accomplishes this by acting on the JFET Q4, establishing, therefore, a triangle-wave of current through Q4's source. Q4 was chosen for its extremely low gate current and extremely low pinch-off current. Since Q4's gate current is neglible, Kirchoff's current law tells us that the drain current will be equal to the source current. Presto! A triangle-wave of current is injected into the resistor network of R_7, R_8, R_9, R_{10}, and R_{12} (dominated by R_{10}), which will cause a triangle-wave summation of voltage at Q4's drain, which R_7 and R_8 will ultimately convert into a triangle-wave of current for summing into the amplifier.

Phew! Why go through all these different stages? Well, the most challenging problem is how to turn OFF the triangle-wave *utterly*, so that it doesn't at all interfere with the normal operation of the amplifier, without using a mechanical switch like a relay. The current-source circuit of U8a and Q4 acts as a switch, blocking the triangle-wave, or letting it pass virtually uninhibited. You may still wonder why the drain of the JFET was not allowed to inject current directly to the summing junction at the inverting-input of U3. Two reasons: 1, any added capacitance at the input to U3 is a potential source of noise and of instability, and 2, the JFET can turn off hard, but not quite THAT hard. The resistor network reduces the sensitivity of the log-amp to the JFET currents, so we can get away with a little bit of leakage.

To turn-off the triangle-wave circuit, SIG_CHAN_TEST must be brought low, which turns on Q7, which turns on Q6, which forces the gate of Q5 to -15V, shutting it off. The triangle-wave at the non-inverting input of U5 is therefore halted, and railed positive. At this high voltage, U8a loses control, and its output hits the negative rail, forcing Q4 off. So now Q4 is off, and the triangle-wave generator is inactive, so all is nice and quiet.

Interface Logic/Timing

Interfacing to the log-amp is straight-forward. There are three addressable devices on-board: the 12-bit signal ADC, the calibration DACs, and the calibration EEPROM. The three device-select lines are present at the 48-pin DIN connector J1 (LOG_AMP*, LOG_CAL_SEL*, and CAL_MEM_SEL*).

The four address LSB's are brought-in to address the EEPROM. Also, ADRS0 is used to select between the two calibration DACs. 16 data bits are brought on-board, as well as the MSE (Mass Spec. Enhanced) Bus READ* and WRITE* strobes.

The two strobes may be used to strobe the EEPROM device-select line CAL_MEM_SEL*. The other two device lines, however, *must* be strobed off-board. Further, the calibration DACs completely ignore the strobes, since it's a write-only device.

2-wait-states (referenced to the 100ns/state ADSP2101 on SmartCard) should be sufficient for reading the ADC (depending, of course, on the bus interface timing of the parent board), which has a maximum read access time of 150ns (typically 75ns), or max. 163.2ns with on-board delays. The EEPROM and calibration DACs need a little bit more time, so a minimum of 3 wait states are required (see the table at the beginning of this document).

ADC: Logic configures the 12-bit signal ADC as a read/write device. A read causes the last converted word to be asserted on the data bus (note that the 4 data MSB's are pulled low, to fill the 16-bit bus); immediately

following the read, a new conversion cycle is initiated. A write (or, equivalently, device-select without asserting READ*) simply initiates a conversion cycle, without fetching any data. Data should be ready to fetch $\geq 10\mu s$ following start-convert. An EOC* (end-of-convert) line is available for use off-board; the EOC* line stays high until the conversion is complete, and may be used off-board for a variety of purposes. On 7UP, it's used to detect a bad log-amp ADC, or missing log-amp board, or possibly an over-zealous sampling rate arising from a firmware bug (this has never been seen).

Calibration DACs: The DACs are write-only devices. To simplify the on-board logic, the WRITE* strobe is not sensed; instead, the write instruction is implicit e with device selection. ADRS0 is sensed to select between the two DACs of U1. The U7 Schmitt-trigger logic, in conjunction with data buffer U4, 'protects' the calibration DACs from switching signals at its inputs at all times except during LOG_CAL_SEL*, to repress digital switching noise. In other words, U1 will not see MSE bus activity whatsoever, except when absolutely necessary.

When LOG_CAL_SEL* is asserted (pulled low), data buffers U4 turn-on, asserting the data bus at U1. Also, ADRS0 is asserted at U1's DAC-select line, as quickly as U7 can propogate the signal (through two gates; max. 18ns total). The RC circuit of R22 and C19 delays final U1 device selection, to compensate for this delay. The required DAC-select set-up time is not specified by U1's (AD7528) data sheets; however, we know we must at least compensate for the 18ns max. propogation time through U7. The RC circuit provides ~35ns of delay, allowing at minimum ~17ns (35ns-18ns) set-up time. When U1 is finally selected, the input data latches become transparent.

When LOG_CAL_SEL* is de-asserted (pulled high), U1 is immediately de-selected, since LOG_CAL_SEL* goes straight to the part, and the data is latched. At the same time, data buffers U4 are turned-off. U1 requires no data hold (this is why the AD7528 remains the choice for U1, not TLC7528, which is an otherwise superior part)[1]. The RC circuit of R30 and C17 provide a good healthly DAC-select hold-time. U1 requires 20ns of hold-time, 30ns across temperature. THIS MEANS THAT ADRS0 MUST REMAIN VALID FOR AT LEAST 27ns (30ns - U7 min. delay of 3ns) FOLLOWING DEVICE DE-SELECT.

EEPROM: The EEPROM can be treated like any read/write device. Writes require jumper P6. For further specifications, see the specification sheet for 1818-5128, 28C64

Special Components

The two most difficult to source components are U3 and Q2, the logging op-amp and the transistor pair.

U3 must have a low input-offset voltage to reduce bias-current errors (through R_7 & R_8), low input bias current (again, to reduce the bias-current error), a high phase margin, and a low noise specification. AD820BR was chosen, which comes pretty close to satisfying all these requirements. TLC2201ACD, from TI, was a candidate, but its phase margin was insufficient, causing the amplifier to oscillate.

[1] !!! In retrospect, we could easily provide data-hold by changing U4 into a latch, instead of simply a buffer, likely without any board spin...?

A nice feature of the AD820BR part is its ability to rebound quickly after slamming into a rail, an event that could be triggered by, say, an ESD event. A quick recovery ensures a minimum of data loss, should such an event occur.

Q2 needs to be a matched PNP pair, with low collector-emitter capacitance. Also the transistor must exhibit a nice 'loggy' response from the pA range through to 50µA. First, the Siemens part BC857SC was chosen, and worked well in the prototypes. Availability became a big issue, so we switched to the Toshiba part HN1A01FU. Neither of these transistors had a matching specification, but they seemed to work out well anyway, the rationale being that since they're on the same die, they must as a consequence be pretty well matched. The PMI part SSM-2220S had high capacitance, which killed the bandwidth, so it didn't work out. The Harris part HFA3128, a 5-transistor array, exhibited an 'unloggy' response for some reason, so it did not qualify. So we have two parts which qualify: HN1A01FU from Toshiba, now the default choice, and BC857SC from Siemens, with the same footprint. A word of caution when switching from one to the other: the nominal calibration points were designed for the Toshiba transistor, so calibration ajustment ranges may not quite be compatible. Also, the capacitance may not be identical, so low-end bandwidth must be re-verified. C_4 may be reduced or removed to increase the bandwidth, if necessary, but watch the noise level and amplifier stability.

Ground Management, Shielding, and Reference Voltages

The 4-layer board is split into two sections. If you look at the underside of the board, you'll see very clearly the division between the digital and analog sections of the board. It's so startingly clear because the under-side has been designated as a power-plane layer, not as a signal layer which is the usual case. The reason for doing this was to provide enhanced shielding for the sensitive front-end of the amplifier, which will very merrily amplify 60Hz noise.

The 'phone-bell' can on the topside and the power-plane on the underside form the top and bottom of the shield 'box'. Around the rim of the can are vias to the shield-ground-plane at fairly close spacing, which provide the 'sides' to the shield 'box'.

The underside plane is split and shared by DCOM and shield-ground. The other power layer is shared by +5V and ACOM. Shield-ground is not used to carry currents, and is connected to ACOM by a trace at the lower-right-hand-corner of the board. Since there are no more power planes left, analog power voltages must travel along thick traces on the two signal layers.

The ADC (U6) provides separate pins for analog and digtal power and for ACOM and DCOM, so we can keep the planes separated as much as possible. Buffers U10 and U11 transmit the ADC output off-board, to reduce the output current requirements of the ADC, hence reducing digital currents within the ADC for better noise performance.

The calibration DAC U1 is protected from digital switching by buffering the data with U4, and by preventing activity on the DAC's select lines by using the schmidt-triggers U7 (here, a picture is worth 1000 words).

References: U6 provides the 10V reference upon which the other references are based. The dual op-amps of U13 create +5V and -5V using precision resistors. Notice that the +5V reference is use as a power supply for

the op-amp U3, and the -5V reference is used solely as a reference. Both U13a and U13b have resistances added to their outputs to protect the op-amps from load capacitance, which could drive them unstable. The draw-back is the amplifier's reduced ability to compensate quickly to load changes, but it doesn't seem to be a problem.

EEPROM Contents

The 8-bit EEPROM is used to store the two calibration numbers (gain and offset), as well as the log-amp revision code. Also a calibration stamp is included to indicate calibration; the stamp is made up of the three ASCII codes 'C', 'A', and 'L', or decimal 67, 65, and 76. A log-amp without this stamp has not passed calibration.

Address Offset	Contents
0	Gain
1	Offset
2	Rev. code
3 →5	Calibration stamp "CAL"
6 →7	Undefined
8 →15	Alpha-numeric serial no., used by Manufacturing

Revision code 0 indicates an old-style 20µA, 2KHz log-amp, with un-log equation:

$$COUNT = 100\left(2^{\frac{ADC}{256}} - 1\right) \qquad (12)$$

Revision code 1 indicates the 50µA, 4KHz log-amp, with un-log equation:

$$COUNT = 370\left(2^{\frac{ADC}{265}} - 1\right) \qquad (1)$$

SmartCard reads this revision code, and generates the un-log table accordingly.

Electronic Board Specifications
G1946, SPRITE
April 21, 1997

1. Introduction

This document outlines the electronics and their interactions with SmartCard and the Host. Most of the sections in the document will briefly describe the electronics and their voltage/current ranges along with the interface between SmartCard and the Host.

There are Five main functions on this board; 1) Mass Axis Drive, 2) Octopole Drive, 3) Low Voltage Lenses, 4) High Voltage Lenses, and 5) Readbacks.

2. Mass Axis Drive

The Mass Axis Drive consists of the Mass Axis DAC, Mass Gain & Mass Offset DACs, AMU Gain & AMU Offset DACs, Quad DC Offset DAC, and Direct Digital Synthesis interface. The following table outlines the relationships of the various DACs.

Parameter	Res. (SW)	Range (SW)	Equation
Mass Axis	0.05 AMU	0 to 3276.75 AMU	DAC = 20 * AMU
Mass Axis Offset	0.01 AMU(PR) 0.002 AMU	-20.0 AMU to +20.0 AMU(PR) -4 AMU to +4 AMU	DAC = 2048 + 100 * AMU(PR) DAC=2048 + 500 * AMU
Mass Axis Gain	0.05 AMU at 3276.75 AMU	-100 AMU to +100 AMU at 3276.75 AMU	DAC = 2048 + 20 * AMU
AMU Offset	1	-2047 to +2047	DAC = 2048 - #
AMU Gain	1	-2047 to +2047	DAC = 2048 - #
Quad DC	0.02 v	-40v to +40v	DAC = 2048 - 50 * Voltage
Quad Frequency	10 Hz	900.00 Khz to 1100.00 Khz	Count = 2^32 * (Freq[Khz]/20000)

The Mass Axis DAC is a 16-bit DAC that controls the AMU setting of the instrument. The Mass Gain & Mass Offset DACs adjust the Mass Axis setting and are used for tuning the peak positions. These adjustments are expressed in units of AMU. The AMU Gain & Offset DACs are used to adjust the peak width settings across the mass range. There is not an accurate relationship between peak width and DAC setting. The Quad DC Offset DAC is used to adjust the relative DC voltage of the quad. Normally the relative DC of the quad is 0 volts. However, experiments have shown that adjusting the voltage to something other than 0 volts can have an improvement in sensitivity and/or resolution. The Quad Frequency is driven by a Direct Digital Synthesis interface (DDS) and is used to "dip" the quad. The DDS interface has a 32 bit count register that sets the frequency. The value of "Count" in the equation column is a 32 bit number.

3. Octopole Drive

The Octopole drive consists of two 12-bit DACs that control the peak amplitude and AMU knee of the 2.4576 MHz amplifier. The peak amplitude is the Peak to Peak voltage between the poles of the Octopole. The following table shows the relationship of the DAC value to AMU setting.

Parameter	Res. (SW)	Range (SW)	Equation
OPOLE PEAK	1 v	0 to 350v p-p	DAC = 8 * Voltage
OPOLE KNEE	1 AMU	0 to 3276 AMU	DAC = AMU

4. Low Voltage Lenses

The low voltage lenses consist of the Fragmentor, Iris, Skimmer 1, Skimmer 2, Ion Energy, Lens 1 and Lens 2. All of these voltages are considered "LOW" voltages because they are +/- 500 V or less. Electronically, they are driven from a bipolar stacked transistor design that offers low current, bipolar operation from common voltage rails. All of the lenses are driven from 12-bit DACs. The lenses are further defined as having a 1V or 0.1V SOFTWARE resolution.

The following table outlines the Host resolution and limits along with the equation that relates Host voltage number to DAC value.

Lens	Res. (SW)	Range (SW)	Equation
Skim1, Lens2	1v	-300v to +300v	DAC = 2048 + 4 * Voltage
Iris, Fragmentor	1v	-450v to +450v	
Skim2, Ion Energy, Lens1	0.1v	-50v to +50v	DAC = 2048 + 40 * Voltage

The equation in the table above assumes that the Voltage is a bipolar value within the range of the lens. If the Host software is providing a Voltage Magnitude and Polarity, then SmartCard should combine the two to make a bipolar value, or use two different equations:

DAC = 2048 + 4 * Voltage for positive polarity.

DAC = 2048 - 4 * Voltage for negative polarity.

5. High Voltage Lenses

The high voltage lenses consist of the Chamber, Capillary, and Corona current. These voltages are considered high voltages because they approach 10 kvolts. In the SPRITE design, the Chamber voltage trails the Capillary voltage, therefore, there is no direct control of the Chamber voltage, hence it will not have a parameter value. The Corona control voltage actually sets a current and not a voltage, but the associated voltage is still high. The following table outlines the relationships of the voltages.

Parameter	Res. (SW)	Range (SW)	Equation
Capillary	50 v	-6000v to +6000v	DAC = Voltage/2.4420

Corona	0.1 uA 0.1 uA	10 uA 100 uA	DAC = 409.6 * Current [uA] DAC = 40.96 * Current [uA] for Neg. APCI

In the above table, the DAC relationships are not integers. The DAC values must be truncated to 12 bit integers.

6. Readbacks

The readbacks on the Analyzer board provide status and voltage/current measurements. The status readbacks are bits that provide a "Failure" or "No Failure" readback. Most of these bits let the firmware know whether or not a circuit is functioning on the board. The voltage and current measurements are "real value" measurements. The values come from a Muxed Analog to Digital (A/D) converter. The following sections describe the functionality of the readbacks.

6.1. Status bits

The status bits provide the firmware with a means to determine the state of the Instrument. Since the bits only give a "1" or "0", their meaning is limited to "Failure" or "No Failure". There are two registers that hold status bit information; 1) Status 1 register, and 2) Status 2 register.

6.1.1 Status 1 register

The Status 1 register is the main register that determines the state of the instrument. The information in this register is latched, which means that any fault that occurs in the system is held in the register until firmware clears that register. The register is cleared by writing to the Status 1 register. Each bit in the Status 1 register has a Mask bit that lets the status bit cause a "shutdown." The mask bits are configured by the Shutdown Mask register. A "shutdown" means that various voltages and functions in the instrument will turn off and go to a predetermined safe state. The following is a list of the Status 1 register bit definitions:

	HED	CDEM	ID		RF			OCTO				DAC CAL	LV LENS	APCI	CAP
15				11				7				3			0

Each bit in Status 1 Register corresponds to a fault or state condition. If the status bit is '1', then a fault has occurred. It the fault bit has a corresponding Mask bit set to '1', then a shutdown will occur. If the status bit is '0', then no faults are occurring and no shutdown will occur from that bit. Each bit is described below.

Bit 0, CAP: The bit will set when the Source High Voltage supply control loop cannot maintain the desired voltage on the Capillary. This may occur due to leakage currents in the source, shorted high voltage lead, driving the supply too high of a voltage, or a hardware failure on the analyzer board.

Bit 1, APCI: This bit will set when the APCI needle supply control loop cannot maintain the desired current on the needle. This may occur due to leakage currents in the source, improper needle position and/or flow rate, broken open high voltage leads, driving the supply too high of a current, or a hardware failure on the analyzer board.

Bit 2, LV LENS This bit will set if the one or all of the low voltage lenses is having a problem driving the correct voltage on the lens. This may be caused by a shorted lens plate, a shorted lens cable, or a hardware problem on the analyzer board. The bit may also set if the low voltage lens supply fails itself. In any case, this is the same as a hardware failure on the analyzer board. If the problem is one of the lenses, status 2 register will provide information as to which lens has a problem.

Bit 3, DAC CAL This bit will set if the Mass-Axis DAC needs calibration. The Mass-Axis DAC has an internal uC that calibrates the gain and offset of the DAC to insure that it is good to 18 bits. The adjustments needed by the DAC are stored in RAM internally in the DAC. If a power glitch or ESD event occurs, the DAC will sense this and assume that the internal RAM is corrupt. It will then issue a signal that causes this fault. Firmware must then recover from the fault and issue a Calibration sequence in the MODE CONTROL register.

Bit 7, OCTO — This bit will set if the Octopole control loop cannot maintain the desired RF voltage on the Octopole. This may occur due to shorted Octopole leads, output transformer needing adjustment, overdriving the RF peak voltage, an Octopole board failure, or an analyzer board failure.

Bit 10, RF — This bit will set if the Quad RF control loop cannot maintain the desired AMU setting. This may occur due to a wrong Quad Frequency setting, failed coil box, failed RF Power Amplifier, shorted or open quad contact leads, insufficient vacuum, hardware failure on the Analyzer board, or any of the cables connecting the various elements together is broken and/or not connected.

Bit 12, ID — This bit will set if the wrong source combination is detected. There are three magnetic relays in the source that determine the type of source connected to the instrument (APCI or ES). If the wrong combination of magnetic relay contacts is detected, then the APCI needle supply will shut off (and will show an APCI fault) and this bit will set. The ID magnetic relays bits are defined in Status 2 register, bits 8, 9, and 10.

Bit 13, CDEM — This bit will set if the control loop for the Electron Multiplier cannot maintain the desired voltage. This may occur due to a shorted detector, shorted CDEM cable, insufficient vacuum, or a hardware failure on the Detector Board.

Bit 14, HED — This bit will set if the control loop for the High Energy Dynode supply cannot maintain the desired voltage. This may occur due to a shorted detector, shorted HED cable, insufficient vacuum, or a hardware failure on the Detector Board.

6.1.2 Status 2 register

The status 2 register contains additional status information about the system. However, this register is not latched and does not need to be cleared. It is simply a running event latch that is constantly updated. The following are the bit definitions.

					S_ID	HV_ID	N_ID	Q_DC	ION_E	IRIS	FRAG	LNS2	LNS1	SK2	SK1

15 0

Bit 0, SK1: This bit is set if the skimmer 1 lens driver cannot provide the proper voltage to the skimmer 1 plate. This may be due to a shorted skimmer 1 lens cable, a shorted skimmer plate in the source, or a hardware failure on the Analyzer board.

Bit 1, SK2: This bit is set if the skimmer 2 lens driver cannot provide the proper voltage to the skimmer 2 plate. This may be due to a shorted skimmer 2 lens cable, a shorted skimmer plate in the source, or a hardware failure on the Analyzer board.

Bit 2, LNS1: This bit is set if the lens 1 lens driver cannot provide the proper voltage to the lens 1 plate. This may be due to a shorted lens 1 lens cable, a shorted lens plate in the source, or a hardware failure on the Analyzer board.

Bit 3, LNS2: This bit is set if the lens 2 lens driver cannot provide the proper voltage to the lens 2 plate. This may be due to a shorted lens 2 lens cable, a shorted lens plate in the source, or a hardware failure on the Analyzer board.

Bit 4, FRAG: This bit is set if the fragmentor lens driver cannot provide the proper voltage to the fragmentor capillary endplate. This may be due to a shorted fragmentor lens cable, a shorted capillary endplate in the source, or a hardware failure on the Analyzer board.

Bit 5, IRIS: This bit is set if the iris lens driver cannot provide the proper voltage to the iris plate. This may be due to a shorted iris lens cable, a shorted iris plate in the detector, or a hardware failure on the Analyzer board.

Bit 6, ION_E: This bit is set if the ion energy lens driver cannot provide the proper voltage to the Octopole center tap output transformer. This may be due to a shorted center tap on the output transformer, a hardware failure of the Octopole board, or a hardware failure on the Analyzer board.

Bit 7, Q_DC: This bit is set if the quad DC driver cannot provide the proper voltage to the quad. This may be due to a shorted U+/U- cable, a hardware failure of the Coil box, shorted quad contact leads, insufficient vacuum, or a hardware failure on the Analyzer board.

Bit 8, N_ID: This bit is the APCI Needle ID. This bit is set if the APCI Needle is positioned properly in the APCI source body. This bit must be set to run in APCI mode. If it is not set, the hardware will automatically shut off the APCI Needle supply.

Bit 9, HV_ID This bit is the Source High Voltage interlock ID. This bit is set when the ES or APCI source is properly closed. If the HV_ID is not set, then an ID fault is set in Status 1 register, bit 12. If the corresponding Shutdown Mask bit is set, then the system will enter a shutdown state and turn the source high voltage supply off.

Bit 10, S_ID This bit is the Source ID. This bit is set if an APCI spray chamber is attached to the source. This bit is cleared if an ES spray chamber is attached to the source.

The Status 2 register can be used to help diagnose problems. If certain faults are occurring, or the system is not performing properly, status 2 register may provide some detailed information about the problem. For example, if the system is not performing properly with very high mass peaks or very low mass peaks, the problem may be the DC drive electronics. If bit 7 is setting when trying to achieve a high or low AMU setting, then the DC drive electronics have failed. The individual lens drivers can also be tested by individually ramping the voltages on the lenses to the min. and max. values. If the corresponding bit sets in the status 2 register, then the lens driver is having problems achieving the proper voltage. If firmware wishes to enter a diagnostic mode to test the lens drivers, then it is recommended to clear the Mask bit for status 1 register, bit 2. This will keep the system from shutting down if a lens failure cause the Low Voltage lens supply to overload and fault. Furthermore, if a shutdown condition is entered, the Low Voltage lens supply will shut off and not provide the voltage needed for the various lens setpoints. This in turn will cause the lens drivers to show faults in the status 2 register. Therefore, if a shutdown condition is entered, bits 0 through 6 are invalid.

The hardware on the Analyzer board has a mechanism that automatically senses the state of the ID bits (8, 9, and 10) and properly shuts off the APCI source and sets bit 12 of Status 1 register. The following table shows the valid combinations of the ID bits that allow proper operation.

HV_ID	S_ID	N_ID	ID Status 1, bit 12	APCI SUPPLY	MODE
0	0	0	1	OFF	INVALID
0	0	1	1	OFF	INVALID
0	1	0	1	OFF	INVALID
0	1	1	1	OFF	INVALID
1	0	0	0	OFF	ES
1	0	1	0	OFF	ES
1	1	0	1	OFF	INVALID
1	1	1	0	ON	APCI

Because the hardware handles the proper ID selection, the firmware only needs to use the ID bits as a means to diagnose a magnetic relay problem or source configuration problem. However, it is important to set the Shutdown Mask bit that corresponds to the ID fault in order to shutdown the high voltage supplies if a customer opens the spray chamber.

6.2 Voltage/Current readbacks

The voltage and current readbacks are direct analog readings sent through an A/D. The A/D used on the Analyzer board is an eight channel muxed A/D. Because it is muxed, firmware must select a channel and then perform a reading of the device. The configuration and reading of the device all occurs at the MUXED A/D memory mapped location of the MSE bus. Writing data values to the device will configure and select the channel. Reading the device will read the conversion of the previous selected channel. The following table outlines the configuration and channels of the device.

Data Value Written	Channel	Relationship [1]
0x0008	APCI Current	Value [uA] = 0.05 * A/D
0x0009	Vcap Voltage	Value [KV] = 0.0392 * A/D
0x000A	RF Drive Level	Value [%] = 0.3922 * A/D
0x000B	CAP Current	Value [uA] = 0.00784 * A/D
0x000C	Chamber Current	Value [uA] = 0.0392 * A/D (ES & Pos. APCI) Value [uA] = 0.392 * A/D (Neg. APCI)
0x000D	APCI Voltage	Value [KV] = 0.0392 * A/D
0x000E	RF Forward Power	Value [W] = 0.3922 * A/D
0x000F	RF Reflected Power	Value [W] = 0.3922 * A/D

Notes:

1. [V] is units of Volts.
   [uA] is units of microAmps
   [KV] is units of KiloVolts
   [W] is units of Watts
   [%] is units of percent
   A/D is the 8 bit digital word (0 to 255)

2. There is a scale of "10" difference for Negative Mode APCI for Chamber Current.

The "Data Value Written" tells the device the mode and channel to start an Analog-to-Digital conversion. After 60 usec, the data is valid and can be read. Therefore, to read a channel, write the appropriate data value to the Muxed A/D address, wait 60 usec and read the value at the Muxed A/D address. Since none of the items are time critical, this method of "writing and reading" could be done in a background process. If the firmware wishes to be more efficient, the "write" operation could occur immediately after reading. In this approach, read the Muxed A/D location and write the next channel. This is a pipeline operation in that the read is the value from the previous channel selection. If firmware is required to monitor the same channel, only one write operation is needed to select the channel. Firmware would then continue to do successive reads to monitor a single channel. The following sections outline the use of the readbacks.

APCI Current: This signal is a direct readback of the current monitor from the APCI supply. This is useful in determining if the APCI supply is correctly setting the current out of the needle.

Vcap Voltage: This signal is a direct readback of the Capillary monitor voltage from the ES supply. This is useful in determining if the ES supply is correctly setting the voltage on the Capillary.

RF Drive Level: The RF drive level is used to monitor the drive for the AC voltage applied to the Quad. The drive level is proportional to AMU setting in that a higher AMU setting causes a larger RF drive level. The RF drive level is also used to "DIP" the quad frequency. The goal is to change the Quad frequency to minimize the RF Drive Level. If the Quad frequency is too high or too low, the RF Drive Level will increase. The best way to "DIP" is too start at a low AMU setting, make Frequency adjustments, then step to a higher AMU setting and repeat the Frequency adjustments. Using the "same channel" mode of operation might make this easier to accomplish.

CAP Current: This signal provides a current reading on the high voltage CAP plate. This is useful in determining the flow and spray of the nebulizer or APCI needle.

Chamber Current: This signal provides a current reading on the high voltage Chamber plate. This is useful in determining the flow and spray of the nebulizer or APCI needle.

APCI Voltage: The APCI supply is a current controlled supply for the APCI needle. When the APCI current is set, a corona forms on the needle to ionize the sample. The corona current is held constant by the APCI supply by constantly adjusting the voltage. If the spray or needle position changes, the voltage will change to keep the same amount of corona current. This readback provides the APCI voltage needed to supply the given current. This readback is also helpful in diagnosing problems with the spray chamber.

RF Forward PWR: This readback provides the RF Forward Power delivered to the Quad. This readback, as well as the RF Drive Level, help determine the DIP of the Quad. This readback can also help diagnose a problem in the RF Drive electronics. For example, if the RF Drive Level is quite large, but the RF Forward PWR and RF Reflected PWR are quite small, then the problem could be the RF Amp.

RF Reflected PWR: This readback provides the RF Reflected Power back from the Quad. This helps determine the efficiency of the RF AMP and DIP of the Quad. If this signal is large, then either the Quad Frequency is wrong or their is a problem in the coil box and/or RF Amp.

7. Initialization and Fault Recovery.

This section will describe the procedure to initialize the electronics and recovery from faults that cause a shutdown of the electronics. Initializaion involves writing to all of the DACs a "proper" value on power-up. After power-up, the DACs are mainly set by the instruments' tune values. Fault recovery is a procedure to recover from an unmasked fault, which are faults that cause an electronic shutdown.

As described in section 6, the bits in status 1 register can cause a shutdown if the corresponding mask bit is set and a fault occurs that sets the fault bit in the status register. Should a shutdown occur, the instrument will automatically go into a safe state. The following table lists the items in the instrument that are set to a safe state during a shutdown:

Item	Shutdown Value	Reason
Mass Axis	0 AMU	-Quad RF and DC voltages are off
Mode Control Register	0x0000	- Octopole is shutoff - Quad Polarity B is selected {by default, no specific reason}
Low Voltage Lens Supply	0 Volts	- All lens are 0 volts { skimmer1, skimmer2, lens1, lens2, ion energy }
Low Voltage Reference	0 Volts	- Iris and Fragmentor are driven to 0 volts
High Voltage Enables	Off	- APCI needle supply disabled { 0 uA, 0 volts } - Source high voltage supply disabled (0 volts CAP and Chamber)
Status 1 & 2 Registers	Held	- Hold event that caused the shutdown. No new events will occur while the system is in shutdown.
HED	0 Volts	- No voltage on HED plate in detector
CDEM	0 Volts	- No voltage on detector horn

Since the instrument is automatically brought to a safe state, firmware need not further shut things off. Furthermore, the Status 1 Register should contain the bit that caused the shutdown to occur, given that the corresponding Mask bit is set. After the fault is properly reported and the instrument is required to run again, firmware needs to only turn on the items listed in the table above. Most of the DACs that control the voltages are not cleared, therefore, most of the DACs do not need to be re-initialized. However, firmware may chose to directly change DACs in the real-time-subsystem by using MSOFF and MSON procedures.

The following table outlines the items of the real-time-subsystem that need initializaion and fault handling.

ITEM	Power-on initialization	MSOFF	MSON	Fault shutdown	Fault recovery
Front Panel	0x0000	< >	< >	?	?
Shutdown Mask	0x748F				
Log amp Gain	(EE prom)				
Log amp Offset	(EE prom)				
Quad freq. reset	0x0000				
AMU Gain	0x0800				
AMU Offset	0x0800				
Mass Gain	0x0800				
Mass Offset	0x0FFF				
Quad DC	0x0800				
Quad freq. init.	(1 Mhz)				
Octopole Peak	0x0000				
Octopole knee	0x0000				
Status 1 (write)					0x0000
Status 2 (write)					0x0000
Mass Axis	0x0000	< off value >	<rest value>	0x0000	<rest value>
Octopole offset (Ion Energy)	0x0800	0x0800	tune value		
Capex (fragmentor)	0x0800	0x0800	tune value		
Iris	0x0800	0x0800	tune value		
Skimmer 1	0x0800	0x0800	tune value		
Skimmer 2	0x0800	0x0800	tune value		
Lens 1	0x0800	0x0800	tune value		
Lens 2	0x0800	0x0800	tune value		
HV1 (ES supply)	0x1000	0x1000	tune value	0x1000	tune value
HV3 (APCI supply)	0x1000	0x1000	tune value	0x1000	tune value
HED	0x1000	0x1000	tune value	0x1000	tune value
EMV	0x0000	0x0000	tune value	0x0000	tune value
Status 1 (write)	0x0000			0x0000	0x0000
Status 2 (write)	0x0000			0x0000	0x0000
Mode Control	Toggle Mass Cal	octopole off	octopole on	octopole off, Toggle Mass Cal	octopole on

The table shows the values and order to load the values. The Power-ON Initializaiton column shows the items that need initialization and their values. The MSON and MSOFF columns show the elements that need to be changed or controlled to properly turn on or off an instrument. The Fault shutdown and recovery columns show the elements that need to be shutdown during a fault and, if enable, turned back on during recover from the fault. The items listed are not dependant on the type of fault. For example, the table shows a "Toggle Mass Cal" operation which can be performed even though a MASS CAL fault did not occur.

The order of events are from top to bottom of the table. During a fault, one would begin a fault shutdown by writing to the HV1 DAC and continue down the list ending with a write to the mode control register. Upon recovery, begin by writing to the Status 1 register and continue down the list ending with a write to the mode control register.